Di Zhu

Tel: (213) 610-3567 • Email: dizhu@usc.edu
EEB-338, 3740 McClintock Ave. Los Angeles, CA 90089

EDUCATION

University of Southern California, Los Angeles, CA, United States — August 2011 - May 2016 (Expected)
- Ph.D. candidate in Computer Engineering — GPA: 3.93/4.0

Tsinghua University, Beijing, China — August 2007 - June 2011
- B.S. in Electrical Engineering — GPA: 90.3/100 (Top 10%)

RESEARCH INTERESTS

- Low power design and temperature-aware management of on-chip networks
- Hybrid energy storage systems for residential use and electric vehicles

SELECTED RESEARCH PROJECTS

Design Optimization for On-Chip Networks — 2012 - present
- Working on developing a power gating scheme that achieves both high power saving and low latency penalty
- Working on a temperature-aware on-chip network design and management scheme
- Identified the NP-completeness of the energy-aware and fairness-aware application mapping problem for chip multi-processors and proposed an efficient heuristic algorithm to solve it
- Presented an efficient mapping algorithm to minimize delay and power for express-channel based NoCs

Hybrid Electrical Energy Storage System (HEES) for Electric Vehicles — 2013 - 2014
- Developed a cost-aware HEES design methodology for electric vehicles with optimal battery bank sizing to minimize everyday operational costs

Design and Control of the Residential Electrical Energy Storage Systems — 2011 - 2013
- Modeled the residential hybrid EES (HEES) system considering cycle efficiency and aging of batteries, conversion circuit power loss, system weight and volume, etc.
- Proposed a design and control methodology for household HEES system to maximize its return on investment

TEACHING EXPERIENCE

- **Teaching Assistant** VLSI System Design B — 2013 Spring, 2014 Fall
- **Teaching Assistant** VLSI System Design A — 2012 Fall, 2013 Fall

PROFESSIONAL EXPERIENCE

Software Engineering Intern — May to August, 2014
R&D, Cadence
- Developed a complete problem formulation and proposed a solution to implement operand isolation to reduce dynamic power consumption

Hardware Engineering Intern — May to August, 2013
Mobile and Wireless Group, Broadcom
- Set up and configured the Oasys RealTime RTL synthesis toolset, working together with Oasys AEs
- Used RealTime to identify and help eliminate the timing bottlenecks, power consumption hotspot, and wiring congestions of memory management unit and video decoder

SELECTED PUBLICATIONS

- Lizhong Chen, **Di Zhu**, Massoud Pedram, and Timothy M. Pinkston, "Power Punch: Towards Non-blocking Power-gating of NoC Routers", to appear in the 21th IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2015.
- **Di Zhu**, Lizhong Chen, Timothy M. Pinkston, and Massoud Pedram, "Temperature-Aware Application Mapping for NoC-Based Many-Core Processors", to appear in the Design, Automation, and Test in Europe Conference (DATE), 2015.
- **Di Zhu,** Lizhong Chen, Siyu Yue, and Massoud Pedram. "Application mapping for express channel-based networks-on-chip," Proc. of Design Automation and Test in Europe (DATE), Mar. 2014.
- **Di Zhu**, S. Yue, L. Chen, T. Pinkston, and M. Pedram. "Balancing On-Chip Network Latency in Multi-Application Mapping for Chip-Multiprocessors," Proc. of Int'l Parallel and Distributed Processing Symposium (IPDPS), May 2014.