Enhancing the Efficiency of Cluster Voltage Scaling Technique for Low-power Application*

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Abstract— **In this paper, a scheme for power reduction based on Cluster Voltage Scaling (CVS) for gate-level design of the VLSI circuits is presented. To increase the power reduction efficiency of the previous CVS techniques, a new low power level-shifter is utilized in the circuit. In addition, the concept of transistor ordering has been used to further reduce the power consumption. This technique shows an average improvement of 7% compared to the previous CVS circuits. The impact of CVS and its modified version on the reduction of short-circuit and leakage power are also discussed.**

I. INTRODUCTION

With the importance of battery-life and reliability of portable products, the low power design of CMOS VLSI circuits has attracted much attention in recent years and numerous research efforts to address various techniques of power reduction [1]. Reducing capacitance, the switching activity, the frequency, the supply voltage of the circuit, are the bases of these techniques.

Reducing the supply voltage, also called Voltage Scaling (VS), has been deemed as the most potential approach for the power reduction [2]. Since lowering the voltage leads to increasing the delay of the circuit, some techniques have been proposed to deal with performance degradation resulting from the voltage reduction. Parallel and pipeline are two well-known architectures to overcome this problem at the Register-transfer Level (RTL) [1]. In the gate-level designs, however, these techniques can not be applied and, hence, the voltage scaling is performed only on the gates off the critical path of the circuit [3]. Using two different supply voltages for the gates leads to large DC leakage currents which occurs when a low-voltage gate is directly drives a high-voltage one. To avoid this problem, a Level Shifter (LS) is used at the interface of a low-voltage and high-voltage gates. Since the LS circuit consumes power and has a considerable delay, minimizing the number of level-shifters is important in the voltage scaling technique. Considering this fact, a few techniques have been proposed to deal with voltage scaling at the gate level [3-6]. The most popular of them is Cluster Voltage Scaling (CVS) [5], in which the level shifters are used just in the front of the primary outputs. Fig.1 shows the idea behind this technique.

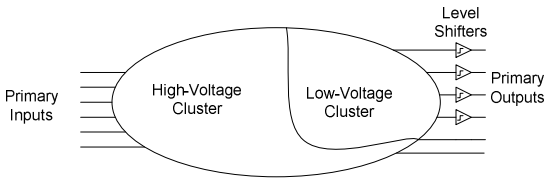

Figure 1. Cluster Voltage Scaling (CVS)

Although CVS uses the least possible number of level-shifters for voltage scaling, the power and delay overhead of the level shifters delimit the efficiency of this technique. Additionally, in most of reported research efforts on CVS, only the impact on the reduction of the dynamic power has been studied and few researches have been deducted to survey the efficiency of this technique for short-circuit and leakage power reduction.

In this paper, a low-power low-delay level-shifter has been incorporated in the CVS technique to reduce the power consumption. In addition, the transistor ordering concept has been utilized in the design. A study of the impact of CVS on the reduction of short-circuit and leakage power components are also presented. The paper is organized as follows. In section 2, we introduce the gate-level model of the power used in this work. Section 3 describes our modifications to CVS, including the low-power level shifter and transistor ordering, while section 4 presents the simulation results and discussion.

II. GATE-LEVEL MODELING OF POWER DISSIPATION

For a comprehensive study on the efficiency of CVS for the power reduction, we need to use some models for describing the power dissipation of the gates .The power dissipation of a CMOS gate consists of three major components: dynamic power, short-circuit power and leakage power. So, the power consumption of a CMOS gate can be expressed by

$$P = P_{Leak} + P_{SC} + P_{Dyn} \quad (1)$$

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where P_{Leak}, P_{SC} and P_{Dyn} are the leakage, short-circuit and dynamic power, respectively and P is the total power dissipation of the gate.

A. Dynamic Power Dissipation

Charge and discharge of load and parasitic capacitances of a gate creates the dynamic power dissipation. With a good accuracy, this component of power can be expressed by [1]

$$P_{Dyn} = \alpha.f.(C_L + C_{\text{int}})V_{DD}^2 \quad (2)$$

where α is the switching activity, f is the clock frequency, C_L is the fanout capacitance, C_{int} is the parasitic capacitances of gate output node and V_{DD} is the supply voltage.

B. Short Circuit Power Dissipation

When the transition time of the input signal of a gate is not short enough, short-circuit power dissipation has a considerable effect on total power dissipation and can not be neglected [8]. Many good approaches have been proposed to address this component of power [see, e.g., 8]. However, the complexity of these models make them not very suitable for a gate-level process. A simple approach for evaluating short-circuit power dissipation which has been proposed in [9] is used in this work.

The short-circuit power dissipation of a CMOS inverter can be expressed as $P_{SC} = f(W_n, W_p, Tr, C_L)$, where W_n and W_p are the widths of NMOS and PMOS transistors, Tr is the 10-90% input transition time and C_L is the load capacitance. In [9] it was shown that with an acceptable accuracy, the short circuit power dissipation of an inverter can be described by

$$P_{SC,r} = \alpha.f.K_r.W_n^{\alpha_{1r}} W_p^{\alpha_{2r}} C_L^{\alpha_{3r}} Tr^{\alpha_{4r}} \quad (3)$$

$$P_{SC,f} = \alpha.f.K_f.W_n^{\alpha_{1f}} W_p^{\alpha_{2f}} C_L^{\alpha_{3f}} Tr^{\alpha_{4f}} \quad (4)$$

where $P_{SC,f}$ is the short-circuit power dissipation when the output of the inverter changes from V_{DD} to 0 and $P_{SC,r}$ is the short circuit power dissipation when its output goes from 0 to V_{DD}. Furthermore, K_r, K_f, α_{1r}, α_{1f}, α_{2r}, α_{2f}, α_{3r}, α_{3f}, α_{4r}, α_{4f} are some parameters depending to the technology and the library. To obtain the short-circuit power dissipation of complex gates (such as NAND and NOR), these gates can be converted to equivalent inverters [9].

C. Leakage power dissipation

In the current technologies, the leakage power consumption is small, but in future technologies this component may have a great impact on the total power dissipation and can not be neglected. In order to survey the impact of any power optimization technique on the state-of-the art VLSI circuits, one needs to consider the impact of this component in the power consumption.

It should be noticed that the leakage power of a CMOS gate not only depends on the gate size, but also on the values of input signals. For example, in a 3-input NAND gate, when all input signals are 0, the leakage power, at least, is one order of magnitude less than other cases [11]. To express the dependency on the input signal pattern, the leakage power of a complex gate when the logical values of its n inputs are b_1, b_2, …, b_n respectively, can be denoted by $P_{Leak}^{State\{b_1 b_2 ... b_n\}}$ [11]. The average leakage power of this gate can be modeled by [11]

$$P_{Leak} = \sum_{b_1 b_2 ... b_n = 00...0}^{11...1} P_{Leak}^{State\{b_1 b_2 ... b_n\}} . \Pr(State\{b_1 b_2 ... b_n\}) \quad (5)$$

where $\Pr(State\{b_1 b_2 ... b_n\})$ is the probability that the logical values of input signals are b_1, b_2, …, b_n, respectively. With an assumption of temporal independence for the input signals, one can write

$$\Pr(State\{b_1 b_2 ... b_n\}) = \Pr(i_1 = b_1).\Pr(i_2 = b_2)...\Pr(i_n = b_n) \quad (6)$$

III. Modification to CVS

A. Level Shifter

As mentioned in the introduction, in the CVS technique, the level shifter must be inserted at the primary outputs to prevent the static current in the circuit. Fig. 2(a) shows the traditional level shifter, called Dual Cascode Voltage Switch (DCVS), which has been used in [2, 3, 5, 6].

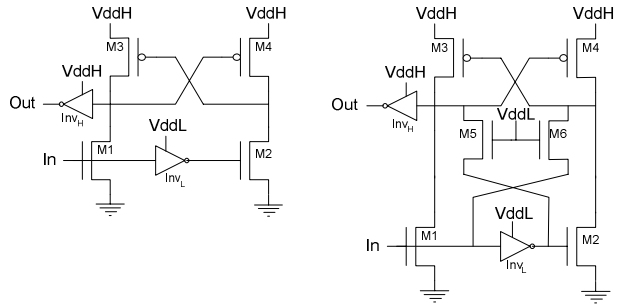

Figure 2. (a) The DCVS level shifter (b) The SDCVS level shifter [12].

Simulation results show that the power consumption of this level shifter is about four to five times that of an inverter. Additionally, the delay of this level shifter is about four times that of an inverter. Thus, it is obvious that using a low power level shifter which has less delay, can improve the efficiency of CVS technique. In [12], a new level shifter has been proposed which has less power and delay at the cost of adding two transistors to the previous structure. This structure, called Symmetrical Dual Cascode Voltage Switch (SDCVS), is shown in Fig. 2(b).

For comparison between this level-shifter and the traditional one, we have simulated both of them by SPICE. The widths of the transistors and inverters with the same name in two structures have been chosen to be equal. Figs. 3 and 4 compare the power and delay of the two structures, respectively. As can be seen, the delay and power of the SDCVS structure is particularly less than DCVS. So, it is expected that the use of this level-shifter can improve the efficiency of CVS.

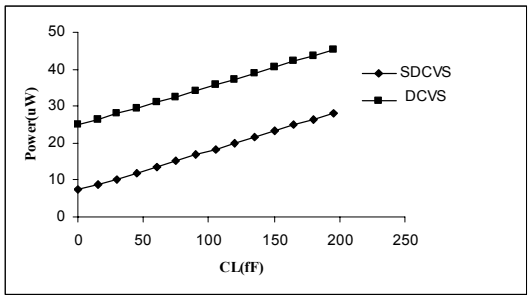

Figure 3. Power dissipation of DCVS and SDCVS level shifters for various C_L.

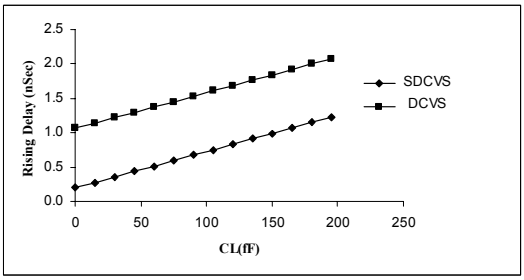

Figure 4. Delay of DCVS and SDCVS level shifters for various C_L.

B. *Transistor Ordering*

At the physical level, it is known that lay-outing the critical-path transistors closer to the output of the gate can result in an increase in the speed of the gate [7] (see Fig. 5). Our experiments showed that with this technique, called Transistor Ordering, the critical time of the circuit could be reduced up to 15%. Using this technique, one can reduce the delay of the circuit in CVS.

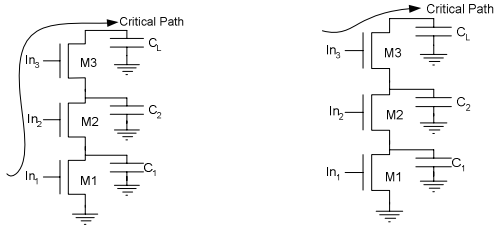

Figure 5. Transistor ordering

IV. SIMULATION RESULTS AND DISCUSSION

For our voltage scaling, we have chosen 3.3V and 2.0V supply voltages. Additionally, for modeling the short-circuit power, we have used HSPICE simulations to obtain the short-circuit power dissipation of an inverter with both high- and low-voltage supply for a variety of parameters (W_n, W_p, C_L, Tr). Then, using Simulated Annealing [10] technique for curve fitting, we have obtained the parameters of (3) and (4) for both V_{DDH} and V_{DDL}. For all cases, the least square error of the fitting was less than 10%. The short-circuit power dissipation of the complex gates in the library was obtained by converting the gates into their equivalent inverters. The leakage power component for each input signal was estimated by simulating the gates of the library for all combinations of the input signal.

We have implemented the CVS technique in C, on the top of SIS [4] environment. In addition, Transistor Ordering feature has been added to the implementation of the CVS. In these experiments, SDCVS has been used at the level shifter. Twenty MCNC benchmark circuits are used as the test bed. Each of them was optimized by "*script.rugged*" provided in the SIS package and then mapped to a minimum delay circuit of the technology library. A 0.35µm CMOS technology library, enriched by adding low-voltage gates, has been used for our simulations.

Table 1 shows a comparison between traditional CVS technique, with DCVS level-shifter and without transistor ordering, and the Modified CVS (MCVS), with SDCVS level-shifter and with transistor ordering. As this table shows the average improvement of MCVS relative to CVS is more than 7%. Table 2 gives more details of our simulations. In this table, we have demonstrated the contribution of short-circuit (SC) and dynamic (Dyn.) power consumption on the power dissipation of each circuit. It is seen that the CVS and its modified version reduce both the dynamic and short-circuit power components. Table 3 shows the number of total gates of original circuit, the number of level-shifters used in CVS and MCVS, and the ratio of V_{DDL} gates in each technique.

The impact of CVS on the leakage power has tabulated in Table 4. As can be seen, in many cases the use of CVS leads to increasing the leakage power. This originates from the fact that the leakage power of a level-shifter (whether DCVS or SDCVS) is particularly more than the leakage power of other gates in the library. So, in future technologies, where the leakage power has a great impact on the total power dissipation, CVS must be incorporated in the circuit with care.

TABLE I. COMPARISON BETWEEN CVS AND MCVS

Circuit Name	Total Power (µW)	Power Reduction CVS (%)	Power Reduction MCVS (%)
rot	748.3	14.21	28.80
apex7	239.7	9.12	14.72
alu2	343.2	0.00	12.73
alu4	675.7	0.22	10.10
i1	64.3	15.15	20.03
i5	206	7.74	10.80
I10	2017	6.00	9.97
term1	202.6	2.44	5.50
c880	444.4	23.05	28.25
c499	527.1	0.00	0.00
c1908	454.5	1.99	8.56
c5315	1766.6	19.21	30.00
my_adder	244.1	0.00	15.43
pair	1780.7	18.46	23.74
k2	390.9	6.04	9.82
b9	121.1	3.42	10.88
x1	325.7	10.59	16.82
x2	49.5	0.00	13.84
x3	851.9	7.63	16.81
dalu	907.8	3.70	7.42
Average		7.45	14.71

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TABLE II. THE EFFICIENCY OF CVS AND MCVS FOR DYNAMIC AND SHORT-CIRCUIT POWER REDUCTION.

Circuit Name	Original Power (μW)		Improvement (CVS)		Improvement (MCVS)	
	Dyn.	*SC*	*Dyn.(%)*	*SC (%)*	*Dyn.(%)*	*SC (%)*
rot	571.3	177	11.85	21.84	25.31	40.05
apex7	182.9	56.8	6.62	17.18	11.32	25.69
alu2	237.3	105.9	0.00	0.00	13.15	11.8
alu4	475.1	200.6	0.13	0.46	9.91	10.53
i1	57.3	7	15.53	12.00	20.42	16.86
i5	171.6	34.4	4.31	24.83	6.58	31.83
i10	1429.5	587.5	4.55	9.51	7.99	14.77
term1	159	43.6	1.89	4.45	4.91	7.66
c880	327	117.4	20.58	29.91	25.93	34.71
c499	387.8	139.3	0.00	0.00	0.00	0.00
c1908	328.2	126.3	1.80	2.49	7.65	10.93
c5315	1295.8	470.8	17.41	24.18	27.92	35.72
my_adder	178.9	65.2	0.00	0.00	15.20	16.04
pair	1308	472.7	19.32	16.07	23.38	24.73
k2	330.6	60.3	4.05	16.92	7.11	24.71
b9	100.2	20.9	3.79	1.63	10.18	14.26
x1	263.8	61.9	10.12	12.57	16.34	18.87
x2	41.7	7.8	0.00	0.00	16.14	1.54
x3	629.6	222.3	5.53	13.57	14.82	22.43
dalu	581.7	326.1	3.59	3.88	8.03	6.34
Average			6.55	10.57	13.61	18.47

TABLE III. COMPARING LEVEL –SHIFTERS AND V_{DDL} GATES IN CVS AND MCVS.

Circuit Name	#Original Gate	CVS		MCVS	
		#LS	*VDDL Gates (%)*	*#LS*	*VDDL Gates (%)*
rot	587	22	29.47	45	58.09
apex7	213	8	23.94	12	32.86
alu2	269	0	0.00	4	15.99
alu4	584	1	0.34	5	12.16
i1	38	4	23.68	6	34.21
i5	198	8	27.27	14	31.82
i10	2077	50	13.10	83	19.40
term1	147	1	6.80	3	13.61
c880	343	15	44.90	20	51.02
c499	518	0	0.00	0	0.00
c1908	467	1	3.64	6	16.49
c5315	1539	34	32.03	48	49.12
my_adder	209	0	0.00	14	47.37
pair	1355	33	26.49	57	36.16
k2	763	14	9.96	25	15.99
b9	98	1	3.06	6	19.39
x1	234	7	22.65	12	33.33
x2	31	0	0.00	2	25.81
x3	602	20	21.26	41	30.40
dalu	926	8	7.13	10	12.20

TABLE IV. LEAKAGE POWER OF CVS AND MCVS

Circuit Name	Org (nW)	CVS (nW)	MCVS (nW)
rot	7.82	7.32	6.91
apex7	3.27	3.18	3.24
alu2	3.31	3.31	2.91
alu4	6.39	6.41	5.79
i1	0.88	0.90	0.94
i5	3.41	3.53	4.11
i10	26.15	26.61	27.54
term1	1.94	1.83	1.83
c880	4.63	3.81	4.00
c499	7.96	7.96	7.96
c1908	7.46	7.34	7.74
c5315	19.22	15.69	14.54
my_adder	3.88	3.88	3.69
pair	15.10	13.91	14.40
k2	9.51	9.83	10.01
b9	1.55	1.52	1.80
x1	2.91	2.61	2.73
x2	0.41	0.41	0.43
x3	4.89	4.71	5.93
dalu	11.33	11.45	11.17