Curriculum Vitae

Kihwan Choi

PhD Student
University of Southern California
Dept. of Electrical Engineering
EE-Systems, EEB330

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Born in Korea (South), 1970

Education

M.S. Electronic & Electrical Engineering, Pohang University of Science and Technology,
Pohang, Korea, February 1994
Emphasis on III-V Semiconductor Device Physics, Process and Characterization
Thesis: Sulfide Treated GaAs MISFETs with Gate Insulator of Photo-CVD Grown P3N5 Film

B.S. Electronics Engineering, Hanyang University, Seoul, Korea, February 1992
Emphasis on Electronic Circuits, Communication, Semiconductor Device, VLSI

Awards and Honors

Scholarship for Ph.D. Degree Abroad, awarded by Samsung, 1999
Graduate School Fellowship, awarded by the Graduate School,
Pohang University of Science and Technology, 1993
Scholarship for Undergraduate/Graduate Students, awarded by Samsung, 1991-93

Papers and Patents

"Floating-well Charge Pump Circuits For Sub-2.0V Single Power Supply Flash Memories"
VLSI Circuits, 1997. Digest of Technical Papers. ,pp 61-62, 1997
"Effects of sulfide passivation on the performance of GaAs MISFETs with photo-CVD grown P3N5 gate insulators", Jpn. J. Appl.Phys., vol.34,Part1,no.2B, pp 1176-1180, 1995
"Effects of sulfide passivation on the performance of GaAs MISFETs with photo-CVD grown P3N5 gate insulators", Int. Conf. on Solid State Devices Materials, pp 619-621, Yokohama, Japan, 1994
"Sulfide treated GaAs MISFETs with gate insulator of photo-CVD grown P3N5 film",
IEEE Trans. Electron Device Lett., vol. 15 no. 7, pp 251-253, IEEE, 1994
"Characteristics of sulfide treated GaAs MISFETs with photo-CVD grown P3N5 gate insulator",
Journal of the KITE, 31(9), p80-84, 1994(in Korean)
"Method for Erasing Data Stored in a Nonvolatile Memory Device"
Pat. No: 5940326 US, pending(JP)
"Charge Pump Circuits having Floating Wells
Pat. No: 5986947 US, pending(JP)
"Method for Erasing Memory Cells in a Flash Memory Device"
Pat. No: pending(US,JP,TW)
"Non-volatile Semiconductor Memory Device and Method of Driving Word Lines"
Pat. No: pending(US,GB,DE,JP,TW)

"Flash Memory Device and Verify Method"
Pat. No: pending(US,JP,TW)
"Non-volatile Semiconductor Memory Device"
Pat. No: pending(US,JP,TW)

and about 30 Korean Patents registered or under examination

PROFICIENCIES

C under MS/DOS & UNIX.
Verilog-XL, OPUS layout (Cadence)
VHDL (Mentor)
HSPICE (Meta)
SYSTEM-HILO (Genrad)
HP4145/4155A (Hewlett Packard)
MS-3400 Series (MOSAID Technologies Inc.)

Professional Experience

05/94-07/00	Senior Engineer Nonvolatile Memory Product Design Memory Product & Technology Division Semiconductor Business Samsung Electronics Co., Ltd.
03/92-04/94	Research Assistant at POSTECH

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09/98-	Design and Analysis : 32M NOR type Flash EEPROM, Samsung
10/97-03/98	Design and Analysis : 16M NOR type Flash EEPROM, Samsung
04/96-09/97	Design and Analysis : 8M NOR type Flash EEPROM, Samsung
05/95-03/96	Design : 128kB EPROM, Samsung for MICOM Embedded memory
07/94-01/95	64M NAND type Flash EEPROM Design and Test, Samsung ; Core Architecture Design for High Speed & Low-Power ; Embedded Erase/Program Logic Design, Synthesis and Verification ; Behavior Modeling of Functional Block with VHDL & Verilog Language ; Develop Efficient Erase & Program Schemes ; Charge Pump Circuit Design for Low-Voltage Operation - Published VLSI Circuits in 1997 and Adopted to all Successive flash EEPROM ; High Voltage Switching Circuit Design ; Reference Voltage Generator Design with Voltage & Temperature Variation Immunity ; Develop Boosting Circuit for Low Voltage Read Operation ; Test & Analysis of Erase/Program Operation of fabricated devices with MS3400 ; Analysis & Optimization of Core Bias Conditions for stable Writing Operation ; Characterization of thin oxide & ONO for Devices Scaling-Down
03/92-03/93	III-V Semiconductor Project: III-V MISFETs Technology Development Pohang University of Science and Technology