Floating-Well Charge Pump Circuits for Sub-2.0V Single Power Supply Flash Memories

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Abstract

Positive and negative charge pump circuits utilizing floating well are introduced. They require simple two-phase clocks and exhibit output characteristics similar to an ideal diode charge pump. The output voltage is directly proportional to the number of pumping stages rather than limited by the body effect as in the conventional circuit. It is demonstrated that the introduced charge pumps can generate enough voltages for typical flash memories even at a supply voltage less than 2.0V.

Introduction

Demand for lower supply voltage(V_{cc}) flash EEPROM is getting stronger as portable applications are widely extended. One of major obstacles in achieving a low V_{cc} flash EEPROM is the internal high voltage generation for program and erase operations. A traditional charge pump circuit, shown in Fig. 1(a), is based on a circuit proposed by Dickson[1] and it is well known that the maximum output voltage is limited by the body effect on the threshold voltage(V_{th}) of pass transistors. It is also shown[2] that utilizing even 0V V_{th} transistor in Fig. 1(a) is not sufficient for sub-2.0V operation. Several modifications from the simple charge pump have been introduced to increase the maximum output voltage by eliminating the body effect at the cost of complicated control circuits, such as a four-phase pulse generator or a boosting circuit [2,3].

In this paper, both positive and negative high voltage generators utilizing floating well configurations are introduced. Due to their unique operating conditions, body effect is completely eliminated with a control circuit as simple as that of traditional two-phase Dickson's charge pump.

Floating-Well Charge Pump Circuits

Fig. 1(b) shows the circuit diagram of the positive floating well charge pump (FWCP). For proper operations with floating well condition, PMOS transistors are used with their body(n-well) floating. During the first phase shown in Fig. 2, the n-well potential of $(i+1)^{th}$ stage, Vwell(i+1), is initially set to Vpp(i)-Vdiode, where Vdiode is the built-in potential of p^+ to n-well diode. Meanwhile, Vpp(i+1) is driven to negative direction simultaneously and the charge transfers through $(i+1)^{th}$ stage PMOS. At the beginning of charge transfer, the source to bulk potential of $(i+1)^{th}$ PMOS transistor is equal to Vdiode (>0V), which means the effective threshold voltage(V_{te}) of the PMOS transistor is even slightly lower than the body-effect free threshold voltage(V_{to}). As a result, the output voltage and the current driving capability of FWCP can be even higher than the conventional body-effect free charge pump circuits. The open-circuit output voltages of N-stage conventional and FWCP can be written as eq. (1) and eq.(2) respectively[1].

$$V_{out(conventional)} = V_{cc} - V_{th}(0) + \sum_{i=1}^{N} [\alpha V_{cc} - V_{th}(i)] \quad (1)$$

$$V_{out(FWCP)} = V_{cc} - |V_{te}| + N[\alpha V_{CC} - |V_{te}|] \quad (2)$$

where $V_{th}(0)$, $V_{th}(i)$ are the V_{th} of the transistor connected to V_{cc} and that of i^{th} stage including the body effect in Fig. 1(a), V_{te} is the effective V_{th} of pass transistors in Fig. 1(b), and α is close to 1 in practical cases. The eq.(1) is valid only when $\alpha V_{cc} - V_{th}(i) > 0$, and the maximum output voltage is limited by the body effect as N increases. Since V_{te} in eq(2) is a constant(~ -0.5V), the output voltage increases as N increases while $\alpha V_{CC} > |V_{te}|$ as shown in Fig. 3. Figure 4 shows measured and calculated output voltage of the positive FWCP circuit with N=6, 10 respectively. Fig. 5 shows the circuit diagram of the negative charge pump circuit utilizing the same floating well concept with NMOS transistors. Each NMOS transistor is fabricated in a separated pocket p-well.

Experimental Results

Fig. 6 shows measured output voltages with positive FWCP and device parameters are summarized in Table 1. It shows 15V is obtainable with N=10 at V_{cc}=2.0V. 15V can be obtained even at V_{cc}=1.5V in case N is increased as shown in Fig.3. No output voltage degradation due to parasitic pnp bipolar transistor is detected up to the junction breakdown voltage of the transistor. Fig. 7 shows measured output current values at a fixed output voltage when N=10. Output current of 121μA at V_{out}=5V is obtained with V_{cc}=2.0V. Considering the measured maximum cell current during CHE(Channel Hot Electron) programming is 350μA, the proposed charge pump circuit can be used to generate enough current with negligible die area consumption for recent high density flash memories.

Figure 8 shows the open-circuit output voltage of negative voltage FWCP when V_{cc}=1.0, 1.5, 2.0V respectively. It shows enough negative voltage (~ -14V) can be generated with 2.0V power supply. The same high voltage can be generated even at lower V_{cc}(<2.0V) simply by increasing the number of pumping stages as in the positive FWCP circuit.

Conclusion

It is demonstrated that the floating well charge pump circuit works like an ideal diode charge pump for wide range of the output voltage. Since the body effect is completely eliminated with the floating well configuration, the necessary output voltage can be obtained even at V_{cc}=1V simply by increasing the number of pumping stages. Both positive and negative high voltage signals with enough current driving capability for typical CHE-programming flash memories can be obtained with proposed circuits even at sub-2.0V single power supply.

References

[1] J.Dickson, IEEE J. Solid-State Circuit, vol.SC-11, pp.374-378, 1976

[2] K. Sawada et al, 1995 Symp. On VLSI Circuits Dig. Of Tech. Papers, pp.75-76.

[3] M. Kuriyama et al, 1992 ISSCC Dig Of Tech. Papers, pp.152-153.

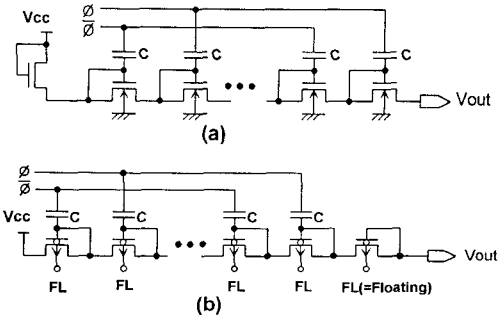

Fig1. (a) Conventional Charge Pump Circuit.
(b) Positive Voltage Floating Well Charge Pump Circuit.

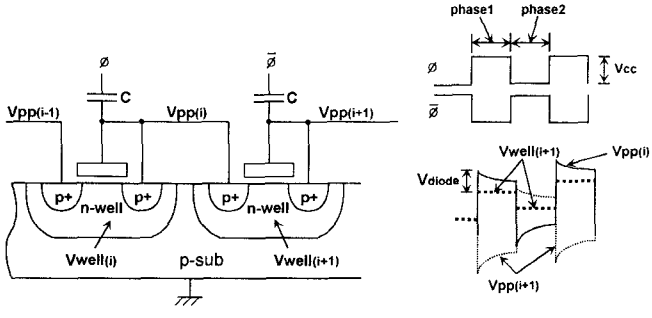

Fig2. Vertical Structure and Internal Signals of Positive Voltage FWCP Circuit.

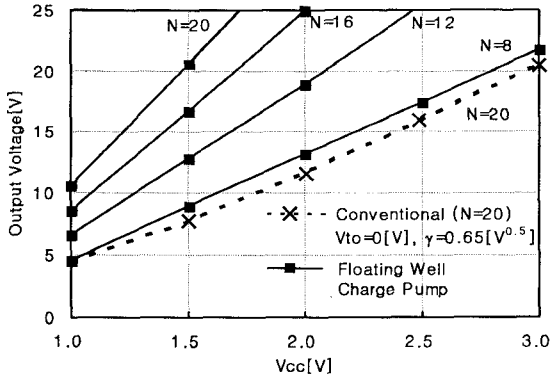

Fig3. Simulated Open-Circuit Output Voltages of Conventional and FWCP.

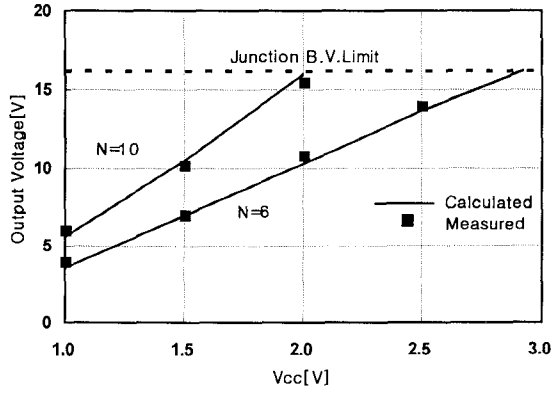

Fig4. Measured Open-Circuit Output Voltage of Positive FWCP.

Table1. Device Key Parameters

Technology	:	0.5μm Triple-Well CMOS 2-layer poly, 2-layer metal
Gate Length	:	1.2μm(High Voltage NMOS) 1.4μm(High Voltage PMOS)
Gate Oxide Thickness	:	25nm
Threshold Voltage	:	0.6V(NMOS), -0.8V(PMOS)

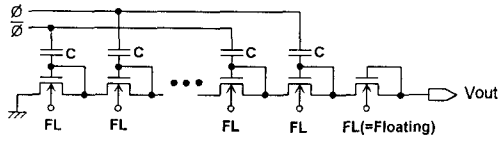

Fig5. Negative Voltage FWCP Circuit.

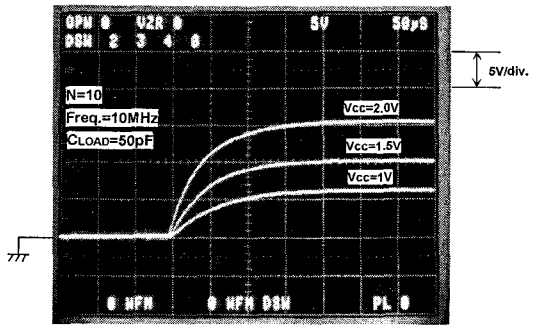

Fig6. Measured Output Voltage of Positive FWCP.

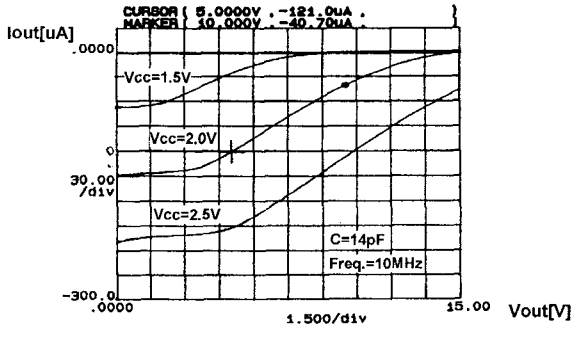

Fig7. Measured Output Current of 10stage Positive FWCP as a Function of the Output Voltage with N=10.

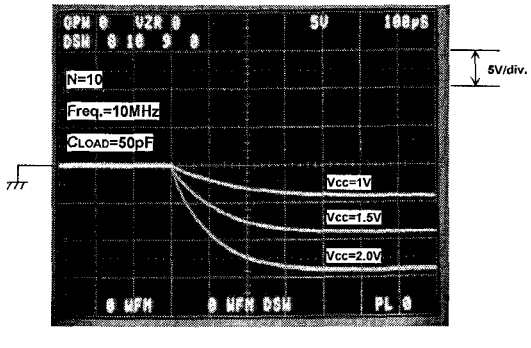

Fig8. Measured Output Voltage of Negative FWCP.