# 10nm Gate-Length Junctionless Gate-All-Around (JL-GAA) FETs Based 8T SRAM Design Under Process Variation Using a Cross-Layer Simulation

Luhao Wang, Alireza Shafaei, Shuang Chen, Yanzhi Wang, Shahin Nazarian and Massoud Pedram
Department of Electrical Engineering, University of Southern California, Los Angeles CA 90089, USA
Email: {luhaowan, shafaeib, shuangc, yanzhiwa, shahin, pedram}@usc.edu

***Abstract*—Gate-all-around (GAA) FETs is proposed as a choice for deeply scaled MOSFETs beyond the 10 nm technology node. In this paper, we present a device and circuit (8T SRAM) co-simulation work based on Junctionless-GAA (JL-GAA) FETs. The same doping concentration level in channel and source/drain can mitigate fabrication complexity and process variability. The 8T SRAM monte carlo simulation results considering process variations shows JL-GAA FETs can reliably operate at low supply voltage.**

***Keywords—junctionless; gate-all-around (GAA); SRAM; process variation; cross layer simulation; current source modeling; monte carlo simulation***

## I. INTRODUCTION

As continuing to scale down the existing MOSFETs beyond 10 nm technology node is challenging due to the short-channel effects (SCE), emerging device structures have been proposed as solutions, such as FinFET [1], gate-all-around (GAA) [2]. Because of the superior gate electrostatic control of the channel, the GAA structure is one of the most promising candidate for the ultimately scaled FETs [3]. On the other hand, changing doping concentration and creating high quality junctions remain as major problems when the fabrication feature size is reaching the sub-10 nm gate length [4]. The junctionless transistors are attracting extensive attentions because it alleviates the abrupt junction formation obstacle and can also provide excellent performance [5]. Using same doping type and concentration level in channel, source and drain can have a simpler fabrication process, reduced thermal budget and less variability. In this paper, junctionless gate-all-around (JL-GAA) FETs 8T SRAM design is investigated under the process variations using a cross-layer framework presented in our previous work. [6, 7].

## II. CROSS-LAYER DESIGN FRAMEWORK

### A. JL-GAA Device Simulation

The JL-GAA device is studied using 3-D Sentaurus TCAD simulation [8] with Fermi-Dirac statistics, density-gradient quantization model and Philips unified mobility model. Fig. 1 shows the 3-D device structure. The gate length ($Lg$), and equivalent oxide thickness ($t_{ox}$) are fixed at 10 nm and 0.68 nm, respectively, according to ITRS specifications for the 11.9-nm technology node. The height ($H_{si}$) and width ($W_{si}$) are 10 nm for achieving a good electrostatic integrity. The leakage current ($I_{OFF}$) is set to 100 nA/μm at 0.5 V by choosing a suitable gate work function ($\Phi_m$ = 4.6/4.68 eV for nMOS/pMOS) and doping concentration level ($8x10^{18}$ and $3.9x10^{18}$ $cm^{-3}$ for nMOS/pMOS). The simulated $I_{DS}$-$V_{GS}$ characteristics for JL-GAA NMOS/PMOS are shown in Fig. 2. JL-GAA FETs are almost fully depleted by tuning the work function of gate material at OFF state, and need relatively high doping for reasonably high drive current at ON state. The performance variations of JL-GAA FETs are believed to strongly depend on doping concentration variation (DV) and work function variation (WFV). Therefore, the DV (σ=~20%) and WFV (σ=~20 meV) are mainly considered as two variation sources in our work. Fig. 3 shows NMOS/PMOS threshold voltage ($V_{th}$) variation distributions due to WFV and DV. The variation parameters can be extracted from fitting the $V_{th}$ distributions using Gaussian function, which are shown in Table I.

### B. Circuit-level Simulation

Based on device simulation, we extract the SPICE-compatible Verilog-A models for fast circuit-level simulations by performing the DC/AC voltage sweeping at terminals. The currents and capacitance values can be stored into a look-up table (LUT). As shown in Fig. 4, the match of DC-AC characteristics of the inverter simulation using both TCAD mixed mode simulation and H-SPICE indicates the accuracy of our LUT based model. Specifically, we use these models in order to measure noise margins, access latencies and energy consumptions, as well as idle-mode leakage power consumption of the 8T SRAM cell (Fig. 5).

## III. RESULTS AND DISCUSSION

Characteristics of the JL-GAA 8T SRAM cell under different supply voltage ($V_{dd}$) levels are reported in Fig. 6(a)-(d). Operating SRAM cell at lower $V_{dd}$ levels reduces the leakage power and access energy consumption, but also increases the sensitivity of SRAMs to process variations. Hence, in order to drive $V_{min}$ (the minimum $V_{dd}$ level with reliable read and write operations), and *DRV* (the lowest $V_{dd}$ level where SRAM can reliably hold the data), we perform Monte Carlo simulations on 1000 samples, and calculate means (μ) and standard deviations (σ) of hold, read, and write noise margins. A high yield SRAM requires a μ/σ greater than 6. Thus, according to Fig. 6(e), $V_{min}$ and *DRV* of the JL-GAA 8T SRAM cell are 0.3V and 0.25V, respectively. At the DRV, 1.94X reduction in the leakage power is obtained.

## ACKNOWLEDGMENT

This work is funded by the DARPA PERFECT program.

## REFERENCES

[1] B. Yu, et al., *IEDM2002*, pp. 251-254. [2] N. Singh, et al., *EDL*, p383-386, 2006. [3] I. Ferain, *Nature*, p310-316, 2011. [4] JP Colinge, et al., *Nature nanotechnology*, p225-229, 2010. [5] CW Lee, et al., *APL*, p053511, 2009. [6] S. Chen, et al., *IEEE S3S conference*, 2014. [7] A. Shafaei, et al., *IEEE S3S conference*, 2014. [8] *Sentaurus device user guide*, Synopsys Inc., Mountain View, CA.

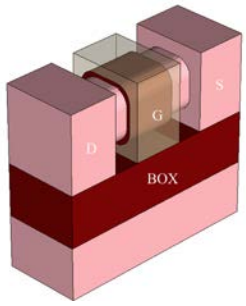


Fig. 1 3D device structure for JL-GAA in TCAD device simulation.

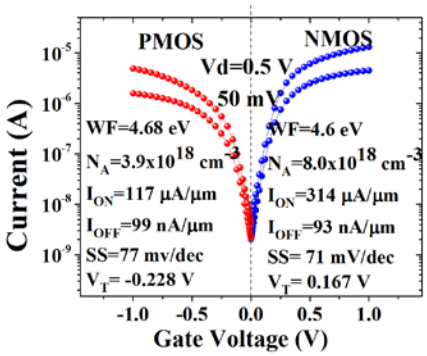


Fig. 2 $I_{DS}$-$V_{GS}$ characteristics of JL-GAA NMOS/PMOS. The performance parameters are measured at $V_{DD}$=0.5 V. Current values are normalized to effective channel width (*Wsi*+*Hsi*) × 2.

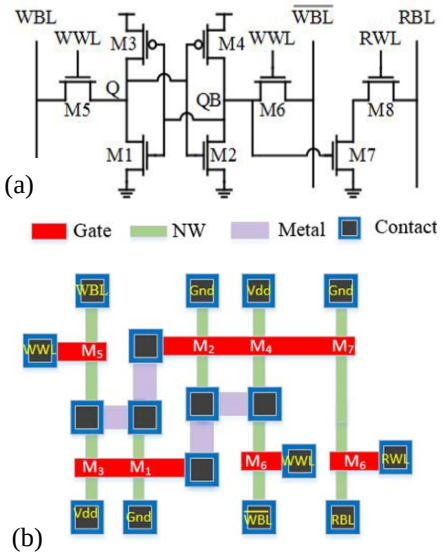


Fig. 5 8T SRAM circuit (a). schematic picture, (b) layout.

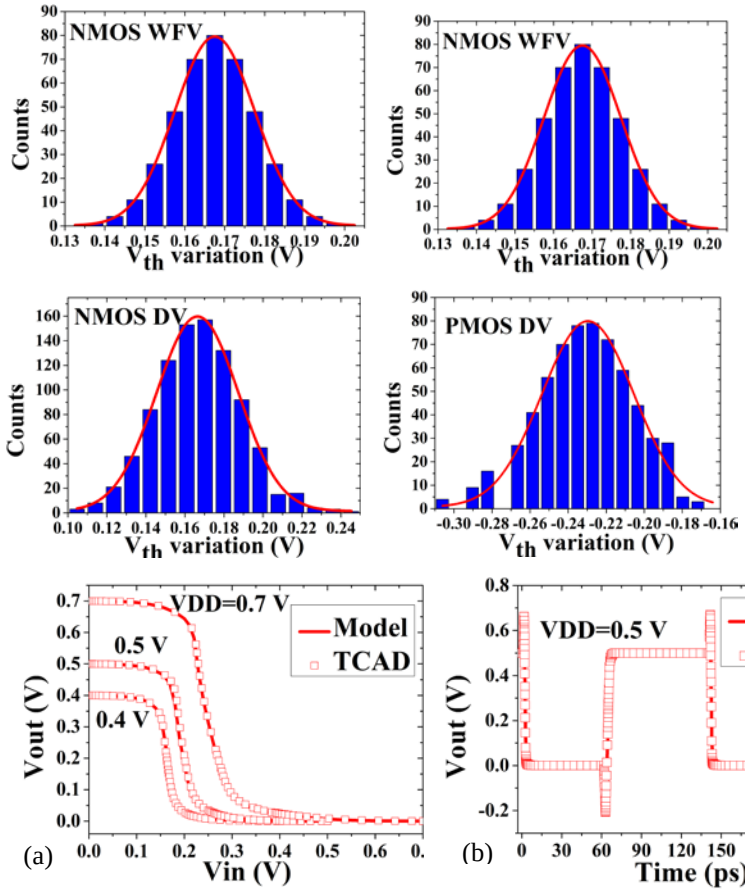


Fig. 3 NMOS/PMOS threshold voltage ($V_{th}$) variation due to work function variation (WFV) and doping variation (DV). The standard deviations of WFV and DV are assumed to be ~20 meV and 20%, respectively.

TABEL I. $V_{TH}$ VARIATION DUE TO WORK FUNCTION VARIATION AND DOPING VARIATION

| | NMOS | | PMOS | |
|---|---|---|---|---|
| | μ | σ | μ | σ |
| Nominal WF (eV) | 4.6 | 0.02 | 4.68 | 0.02 |
| Nominal Doping ($cm^{-3}$) | $8x10^{18}$ | 20% | $3.9x10^{18}$ | 20% |
| Vth variation due to WFV (mV) | 167 | 11 | -227 | 31 |
| Vth variation due to DV (mV) | 167 | 21 | -230 | 24 |

Fig. 4 Inverter simulation (a). DC (at VDD=0.4, 0.5, 0.7 V) and (b). transient response (at VDD=0.5 V) comparison between verilog-A based H-spice simulation and TCAD mixed-mode simulation. The number of channel of NMOS and PMOS are both unit sized.

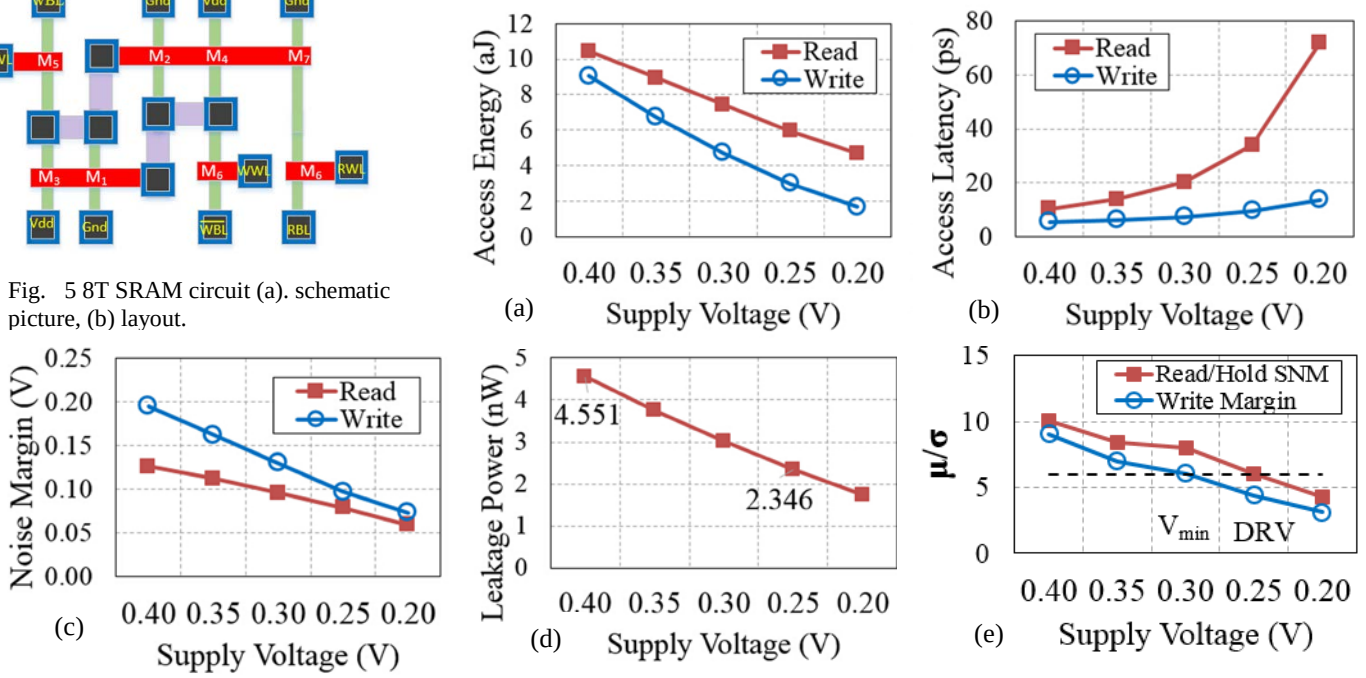


Fig. 6 8T SRAM design simulation at different supply voltage. (a). access latency; (b). access energy; (c). noise margin; (d). leakage power; (e). Hspice monte carlo variation simulation. The sample number is 1000.