High-Performance and High-Yield 5 nm Underlapped FinFET SRAM Design using P-type Access Transistors

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Abstract

In this paper, different characteristics of SRAM cells based on 5 nm underlapped FinFET technology are studied. For the cell structures, which make use of P type access transistors and pre-discharging bitlines to "0" during the read operation, the read current and write margin (WM) are improved. In addition, 8T structures with less underlap for write access transistors are suggested. These structures may have P or N type write access transistor (denoted by 8T-P or 8T-N, respectively). In these structures, using more underlap for the pull down (pull up) transistors of the structures with the P type (N type) access transistors and doubling the fins of the write access transistor may improve the WM significantly without any adverse effect on the read SNM. The results of HSPICE simulations show about 50% improvement for the write margin. Also, the effects of the process variation on various characteristics are investigated. It is revealed that the proposed 8T-P has a WM cell sigma higher than six for supply voltages as low as 0.25 V.

Keywords

SRAM, underlapped FinFET, 5 nm, asymmetric S/D, yield, power.

1. Introduction

Scaling of conventional CMOS technology has increased the density of the transistors as well as their speed. The scaling, however, aggravates the impacts of the process variation and transistor short channel effects (SCEs). In the case of SRAM cells, which are usually fabricated using minimum-sized transistors, the read and write stabilities could be adversely affected by the process variation. The use of new technologies is one of the solutions to suppress these effects. Among different new technologies, FinFET is considered as one of the most promising options to replace the traditional bulk CMOS technology [1]. Based on this technology, some solutions for mitigating the problems of the SRAM cells at the device level have been suggested (see, e.g., [2-4]). In this device structure, using underlapped transistors might mitigate SCEs and improve transistor characteristics such as the ON to OFF current ratio [2]. Moreover, the use of asymmetric transistors results in simultaneous enhancement of the read and write stabilities [3, 4]. Additionally, at the circuit level, to improve both read and write stabilities, the use of topologies which isolate the read and write operations has been proposed [5]. While the circuit solutions might be independent from the device technology, their efficiency will be improved when used with the FinFET technology.

In this paper, different characteristics of 6T and 8T SRAM cell structures implemented using a 5 nm underlapped FinFET technology are studied. The study is performed based on a 5 nm FinFET model recently released for SPICE simulations [6]. The transistors in this model feature different underlaps. The structures include the cells with P type access transistors which have improved read current and write characteristics without increasing the area. The rest of the paper is organized as follows. In Section 2, the device structure and characteristics of the underlapped FinFET transistors are explored while in Section 3, the 6T with asymmetric underlapped transistors and 8T SRAM cells are described. The proposed structures are described in Section 4. The results are discussed in Section 5 and the paper is concluded in Section 6.

2. Device Structure and Characteristics

The term "FinFET" was used for the first time by Berkeley university researchers to describe a non-planar, double gate transistor which was fabricated on a SOI substrate [7]. The main obvious feature of FinFET is a channel made of thin layer of silicon, which is named "Fin". The three conducting gate wrapped around the fin provide a better control over the current passing through the channel. Figure 1 shows a top view of an N type FinFET. Usually in FinFETs, source and drain regions are heavily doped, but the channel is left undoped. Almost a distinct border could be considered between the channel and the drain (or the source). The interval between the border and the oxide edge, if extended to source or drain side, is called "Underlap". The technology used in this work includes three types of devices. The first and the third types are symmetric devices with 1.1 nm and 1.6 nm underlap at both source and drain regions, respectively. The second type is an asymmetric device with 1.1 nm underlap at one side and 1.6 nm underlap at the other side. Note that in practice, the more underlapped side could be at the drain or at the source side. Therefore, there are four modes, two symmetric and two asymmetric (see Table 1), for the device characteristics. The device parameters of the technology are listed in Table 2.

The I_d-V_{gs} characteristics for the devices are presented in Figures 2 and 3 for the saturation and linear regions, respectively.

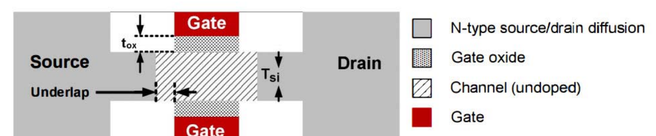


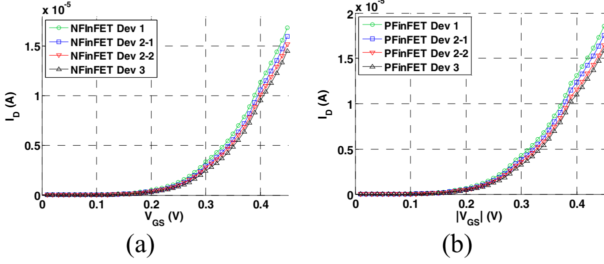
Figure 1. FinFET transistor top view [8].

Table 1. Four modes of the underlapped devices [6].

Name	Source side underlap (nm)	Drain side underlap (nm)
Dev 1	1.1	1.1
Dev 2-1	1.1	1.6
Dev 2-2	1.6	1.1
Dev 3	1.6	1.6

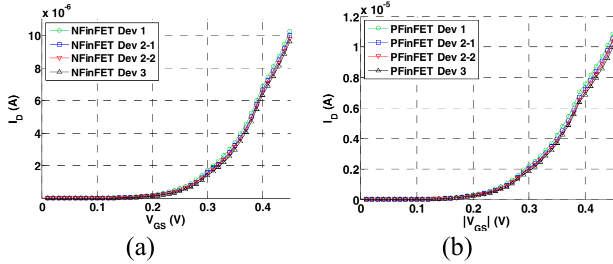
Table 2. Device parameters for transistors [6].

Parameter	Value
Gate physical length	4.9 nm
Oxide thickness	1.1 nm
Fin thickness	2.7 nm
Fin height	10.9 nm
Source/Drain doping	$10^{20}/cm^3$
Supply voltage	0.45 V



(a) (b)

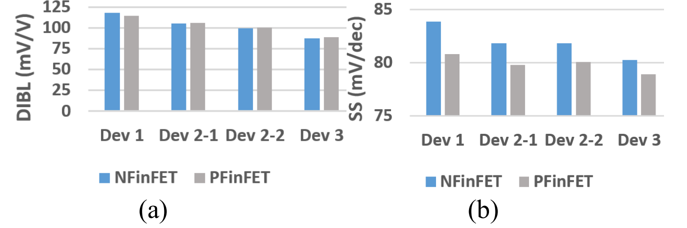
Figure 2. Drain-source current versus gate-source voltage for devices with different underlaps in the saturation region (V_{ds} = 0.45 V) for (a) NFinFETs and (b) PFinFETs.



(a) (b)

Figure 3. Drain-source current versus gate-source voltage for devices with different underlaps in the linear region (V_{ds} = 0.1 V) for (a) NFinFETs and (b) PFinFETs.

The presence of the underlap in the FinFET transistor creates an extra potential barrier for the electrical charges traveling from the source to the drain. Hence, the larger the underlap is, the higher the potential barrier will be. Also, the increase in the underlap enlarges the effective channel length. As a result, the drain current decreases as the underlap increases. For the asymmetric transistors with more underlap at the source side, the current is smaller compared to the case with more underlap at the drain side. The reason is that the lower (higher) field at the source (drain) side cannot (can) lower the extra barrier at the source (drain) side. Therefore, the drain current of the transistor with more underlap at the drain side is higher than that of the other asymmetric transistor. Also, note that the difference in the drain currents of the structures increases with the drain-source voltage [3].



(a) (b)

Figure 4. (a) DIBL and (b) subthreshold swing values for different devices.

As mentioned before, scaling down the channel length worsens the short channel effects including the threshold voltage decreases by increasing the drain voltage. To assess the strength of this phenomenon, the parameter drain induced barrier lowering (DIBL) is used. This parameter is calculated by dividing the threshold voltage difference by the drain voltage difference in the saturation and linear regions as [9]

$$DIBL = \frac{Vt_{lin} - Vt_{sat}}{Vd_{lin} - Vd_{sat}} \quad (1)$$

The DIBL values for different devices are shown in Figure 4 (a). As is expected, more underlap leads to less DIBL values. Again, for the two asymmetric devices, the less values are for more underlap at the source side [3].

The next parameter of importance is the subthreshold swing (SS) which indicates the ability to turn off the device effectively. The SS is defined as the amount of the gate-source voltage needed for a 10 times increase in the drain current. To extract the SS, the gate-source voltages of V_1 and V_2 of the transistors for the drain currents of 200 and 2000 nA were determined. Then, the SS was obtained from

$$Subthreshold - Swing\ (SS) = \frac{V_1 - V_2}{\log\left(\frac{I_1}{I_2}\right)} = \frac{V_1 - V_2}{\log(10)} = V_1 - V_2 \quad (2)$$

The SS values for the transistors are plotted in Figure 4 (b). Again as the underlap increases, the SS value decreases [3].

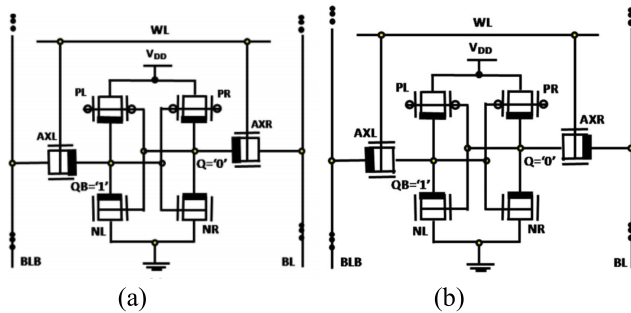
3. Previous SRAM Cell Structures

In this section, we review two previously proposed structures which made use of the asymmetric devices to improve the SRAM cell characteristics [3]. The structures were called 6T-NCUS and 6T-NCUB. In addition, here we consider the 8T cell structure suggested in [5]. The cell used two read access transistors for separating the read and write operation paths. The cell area, however, is larger by about 30% compared to that of the 6T structure [5].

Figure 5 (a) shows the schematic of 6T-NCUS [3]. The more underlapped sides of the access transistors face the SRAM storage nodes (Q, QB). Based on the discussion given in Section 2, the underlap causes an extra potential barrier between the source and the drain. When the extra barrier is at the drain side, due to the high field, the barrier height is reduced and transistor acts more like a transistor without the underlap. When the barrier is at the source side, because of low field at the source side, the potential barrier height remains more or less unchanged. The 6T-NCUS structure takes advantage of this feature. During the read operation usually two bitlines are pre-charged to “1” and by

switching access transistors ON, the cell value is written on the bitlines. The key note is that the cell value must not change during the

read operation. This means that the voltage increase of the "0" storage node must not be more than the trip point voltage (where the two storage node voltages cross each other) of the opposite side inverter. For this reason, the pull down transistors should be stronger than the access ones. Generally, the read operation is performed by discharging the bitline connected to the "0" storage node. During the read operation, the corresponding access transistor would have "0" at the more underlapped terminal. Based on the explanations given in Section 2, this leads to a reduced driving capability for the access transistor, and thus increase in the read stability [3].



(a) (b)

Figure 5. Schematics of (a) 6T-NCUS and (b) 6T-NCUB structures [3]. Thicker lines indicate bigger underlap terminals.

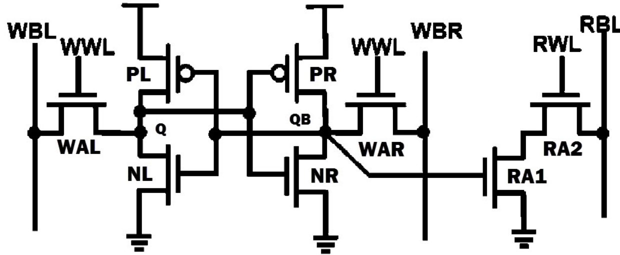
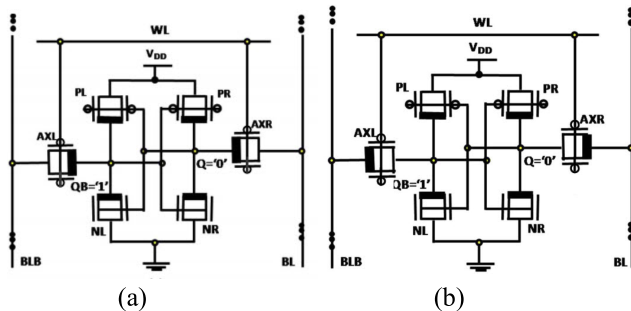


Figure 6. Schematic of the 8T structure [10].



(a) (b)

Figure 7. Schematic of the proposed (a) 6T-PCUS and (b) 6T-PCUB structures. The thicker lines indicate larger underlap terminals.

The write operation is mainly performed from the storage side holding "1" and the corresponding bitline would have "0" value. Because "1" storage node is at the more underlapped side of the access transistor, the extra potential barrier is reduced and driving capability of the transistor is increased. A stronger access transistor would result in a higher write-ability [3].

The other structure introduced in [3] was 6T-NCUB whose circuit schematic is given in Figure 5 (b). In this configuration, more underlapped sides of the access transistors face bitlines. Based on the arguments made in Section 2, the placement of the more underlapped terminals near to the bitlines increases the driving current of the access transistor in the read mode, while decreasing it in the write mode. Thus, its read and write stabilities are lower than those of the 6T-NCUS [3].

An 8T structure, which is proposed in [5], is shown in Figure 6. The hold and write modes are similar to those of the conventional 6T structure. In the read mode, the data is read by pre-charging RBL to "1" and asserting RWL. The basic property of this structure is the connection of the storage node QB to the gate of the access transistor during the read operation. This causes no current flow to the storage nodes, and hence, one does not need to worry about the read stability and cell data flipping. In this cell, the write (read) access transistors are denoted by WAR and WAL (RA1 and RA2).

4. Proposed SRAM Cells

The proposed 6T structures in this work are shown in Figure 7. The key difference between these structures, which are called 6T-PCUS and 6T-PCUB, and the corresponding structures of 6T-NCUS and 6T-NCUB is using P type access transistors. The use of P type access transistors has been suggested in [11] where the cell was implemented using independent gate FinFETs. Here, we suggest using tied gate FinFETs. If the bitlines are pre-charged to "1" during the read operation, the source-gate voltage of the access transistors will be equal to V_{dd}. This increases the drain current of these transistors deteriorating the read stability. To overcome this problem, it is suggested to pre-discharge bitlines to "0" instead of "1". This way the read operation is performed from the side storing "1". In this case, for the 6T-PCUS cell, the more underlaps at the source side of the access transistors forms a weaker transistor increasing the read stability. In addition, the write operation is mainly performed from the side storing "0" which implies that the larger underlap occurs at the drain side of the access transistors inducing higher drain current, and hence, better write-ability. The situations are opposite in the cases of the 6T-PCUB cell degrading its stability during the read and write operation.

As mentioned before, the 8T structure provides isolated read operation and high read stability. These features enable us to improve the write characteristics of the cell without considerably degrading the read characteristics. In order to increase the write-ability, it is suggested to use the strongest transistor for the write access transistors and the weakest one for the pull up (pull down) transistor in the case of cells with the N type access transistors (the P type access transistors) [3]. Based on these suggestions, we introduce two configurations which are 8T-N-1Fin and 8T-P-1Fin. The 8T-N-1Fin (8T-P-1Fin) cell has the N1 (P1) type write access transistors and the P3 pull up (N3 pull down) transistors. It should be noted that the 8T-N-1Fin has the N1

pull down transistors and 8T-P-1Fin has the P1 pull up transistors. These designs increase the write stability while the read stability is not unaffected much due to the isolated read operation. For further improvement in the write stability, we suggest to increase the fin number of the write access transistors to two. This enlarges the strength of these transistors resulting in more write-ability, while it does not have any impact on the area if the spacer pattern technology is used [12]. In this technology, the fins are formed using spacer layers deposited around a sacrificial layer. The technology provides even number of fins. One of the fins is etched away if odd numbers of fins are required. We denote these two new cells by 8T-N and 8T-P. It should be noted that in the case of the 6T cells, increasing the write-ability gives rise to the read stability decrease.

5. Results and Discussion

In this section, to evaluate the efficacy of the proposed SRAM cells, their characteristics are compared with those of the other structures. All the cells were implemented using the 5 nm FinFET technology introduced in Section 2. The results are labeled differently for different structures. The label 6T-N1 indicates a conventional 6T structure with Dev 1 type transistors (see Table 1) and N type access transistors. Similarly, 6T-N3 has Dev 3 type transistors and N type access transistors. 6T-P1 and 6T-P3 are just like two previous structures except for using the P type access transistors. The labels for other cells were the same as used in Sections 3 and 4. Also, the results for the read operation, when the cell had P type access transistors, were obtained for two different modes of pre-discharging bitlines to "0" and pre-charging bitlines to "1". For example, 6T-PCUS-0 represents the results for the 6T-PCUS structure when bitlines were pre-discharged to "0" during the read operation. There is no such classification for the structures with N type access transistors as the bitlines were only pre-charged to "1" for all the structures.

5.1. Nominal Study of the 6T Cells

The read SNM is usually used to characterize the read stability [13]. Figure 8 shows the read SNM values for different 6T structures. As shown in the figure, the structures with the P type access transistors and pre-charged bitlines to "1", have almost zero SNM values. This is justified by noting that the P type transistors transfer strong "1" and weak "0". For the case that the bitlines are pre-charged to "1", when the P type access transistors are turned on, "1" may be easily written into the storage node holding "0" toggling its current value during the read operation (occurring read failure). One way to solve the problem is to make the pull down transistors stronger. For instance, by considering 3 fins for the pull down transistors in the 6T-P1-1 configuration, the read SNM increases to 64.6 mV. This, however, increases the size of the cell. Due to this problem, other results for these cells will not be presented. In the case of our proposed structures, the read SNM values are acceptable. Since the technology used in realizing these cells has stronger P type transistors compared to the N type ones, the read SNM values are slightly lower than the corresponding ones based on the N type pass transistors. Also, note that for larger underlaps, since the channel length effectively increases, threshold voltages becomes larger too. Based on the read SNM equation presented in [13], the threshold voltage increase would improve the read SNM. In addition, the 6T-NCUS (6T-PCUS) cell has a weaker access transistor in the read mode and consequently a higher read SNM (see Sections 3 and 4).

The read current is used as an indicator for the read access time [14]. The read currents for the structures are given in Figure 9 which reveals the structures with P type access transistors have higher read currents. This is attributed to the lower threshold voltage for these transistors in this technology. Also, the channel orientation of the FinFET devices is typically (110) resulting in comparable hole and electron mobilities [14]. As the underlap increases, the threshold voltage increases reducing read current. In addition, 6T-NCUS (6T-PCUS) has a lower read current compared to that of 6T-NCUB (6T-PCUB). This is due to the weaker access transistors for the former during the read phase.

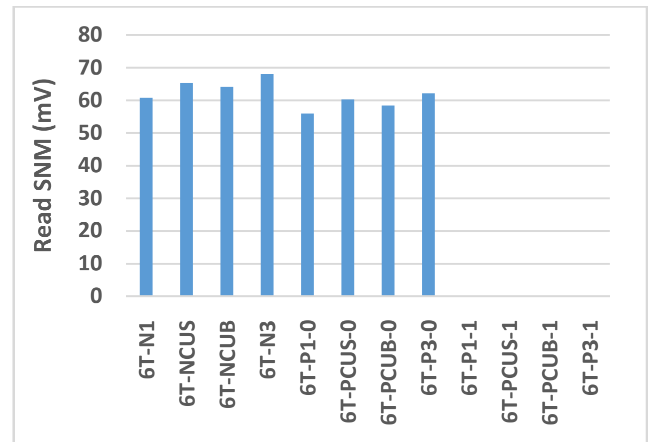


Figure 8. Read SNM for different 6T cells.

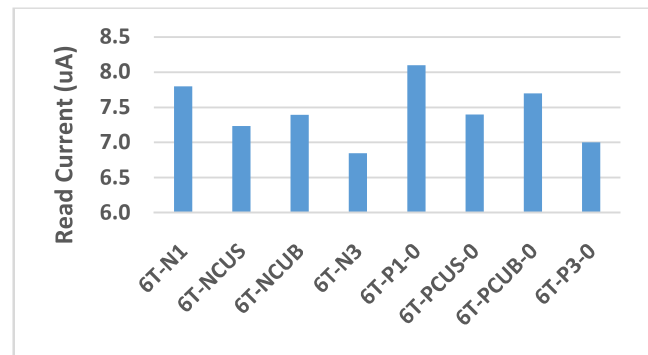


Figure 9. Read current for different 6T cells.

Figure 10 shows the static power consumption for the 6T cells. The static power constitutes the major part of the SRAM cell power dissipation in the current technologies [15, 16]. Due to the smaller threshold voltage of P type FinFETs, the static power slightly increases for the structures with the P type access transistors. On the other hand, the transistors with more underlaps have larger thresholds and lower leakage currents. Also, 6T-NCUS (6T-PCUS) has a lower hold power compared to that of the 6T-NCUB (6T-PCUB), due to the weaker OFF state access transistor. In the case of the dynamic power, for each read or

write operation, the wordline should be activated and then deactivated to come back to the hold state. Since the power is drawn from the supply voltage only during the zero to one transition and the number of these transitions is the same for all the structures, the power consumptions should be the same. With a similar reasoning the bitline voltage changes for the structures consume the same dynamic power.

A stability parameter for the write operation (write-ability) is the Write Margin (WM). There are different definitions for the WM. In this work, we use CWLM [17] whose values for the structures are given in Figure 11. The more threshold values for the underlapped transistors make the cell more resistant to the cell value change. This decreases the cell write-ability and WM. Furthermore, during the write mode, 6T-NCUS (6T-PCUS) has stronger access transistors than their corresponding pull-up (pull-down) transistors providing higher WM compared to that of 6T-NCUB (6T-PCUB).

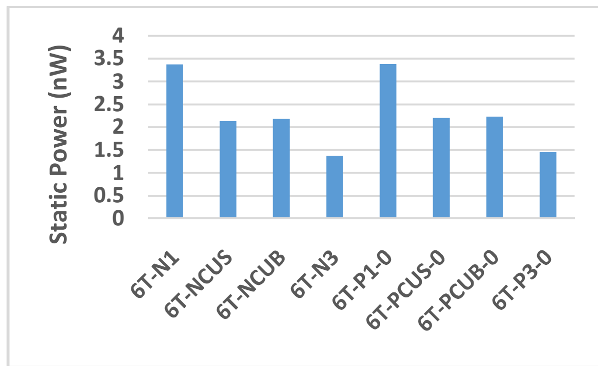


Figure 10. Static power for different 6T cells.

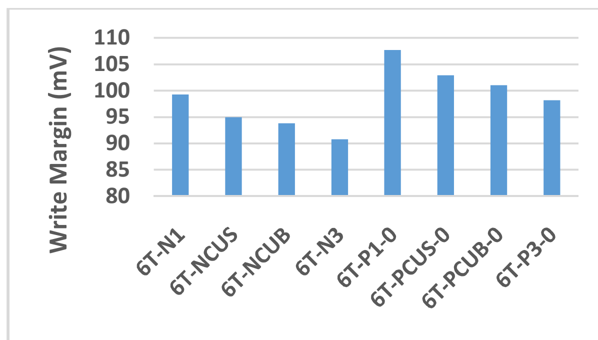
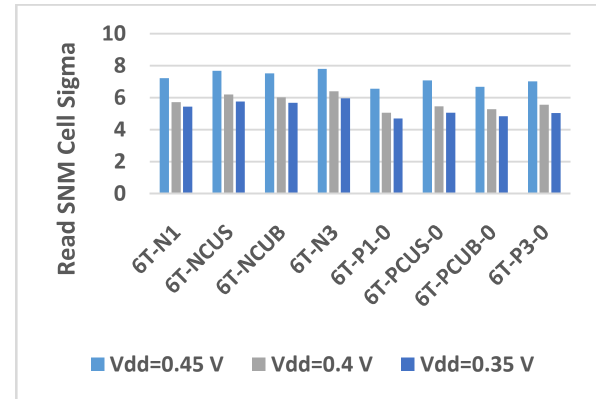


Figure 11. WM values for different 6T cells.

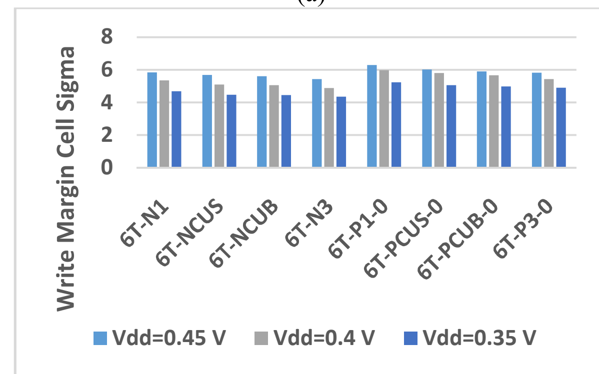
5.2. Study of Process Variation Effect on 6T Cells

To investigate the impact of the process variation on the cells, we used Monte Carlo simulations. For this investigation, we used a random Gaussian variable for threshold voltage of each cell transistor. The variable had a variation of 20% (3σ = 20%) of its nominal value which was used to obtain the cell characteristics. The cell sigma (μ/σ) values of the read SNM and WM at three supply voltages for different structures are given in Figure 12. Note that large SRAM arrays require six or higher cell sigma values [18]. Comparing the relative values of these parameters for the structures, one observes that both the read SNM and WM cell sigma values follow similar comparative behaviors as those of their nominal values presented in Section 5.1.

In the case of the read SNM (Figure 12 (a)), all the values are higher than six at V_{dd} = 0.45 V. Also, all of the structures with the P type access transistors have cell sigma values below six for the supply voltages of 0.4 and 0.35 V. Among different structures, 6T-N3 has the cell sigma above six for all the three voltages. On the other hand, all the structures with the N type access transistors have write cell sigma values lower than six. The 6T-P1 has the cell sigma value higher than six even at V_{dd} = 0.4 V. In addition, 6T-PCUS has cell sigma equal to six for V_{dd} = 0.45 V. In the next section, we discuss the 8T cell which may provide a better write characteristic.



(a)



(b)

Figure 12. 6T (a) read SNM and (b) WM cell sigma (for 0.45, 0.4 and 0.35 V supply voltages).

5.3. 8T Cell Characteristics

Now, we study the effect of the process variation on 8T structures. Figure 13 presents the read SNM and WM cell sigma of the proposed 8T-N-1Fin and 8T-P-1Fin introduced in Section 4 for the three supply voltages. As shown in Figure 13 (a), all the values for the read SNM cell sigma are much more than six in the presence of the process variation. This is due to the fact that the 8T cells have much more read SNM compared to those of the 6T structures. On the other hand, the results shown in Figure 13 (b) reveal higher WM cell sigma values. As a result, the minimum supply voltage for 8T-N-1Fin and 8T-P-1Fin cells (considering the minimum required six cell sigma requirement) are 0.45 and 0.4 V, respectively. As discussed in Section 4, for further improvement in the write stability, we suggest to increase the fin number of the write access transistors to two

(denoted by 8T-N and 8T-P). Next we compare the characteristics of these structures (8T-N and 8T-P) with the 8T cells which use the 6T structures discussed in Sections 3 and 4. For these cells, the types of read access transistors are presented in Table 3. The nominal characteristic of these cells plus the proposed 8T-N and 8T-P cells (totally 10 structures) are demonstrated in Figure 14 to Figure 17. In order to have a better comparison, the numbers of fins for the access transistors of all other eight structures were increased to two. In terms of the read SNM, 8T-N3 and 8T-P3-0 have the highest values while 8T-N1 and 8T-P1-0 have the lowest values. Other cells have more or less the same read SNM values. For the read current, 8T-N1, 8T-P1-0, and 8T-N have the largest read currents. The lowest read current belongs to 8T-N3, 8T-P3-0, and 8T-P. The lowest hold powers belong to 8T-N3 and 8T-P3-0 when the largest hold power are for 8T-N1 and 8T-P1-0. When comes to the write margin, we observe that proposed 8T-P, 8T-P1-0, and 8T-N have the highest write stabilities while 8T-N3, 8T-NCUS, and 8T-NCUB have lowest stabilities.

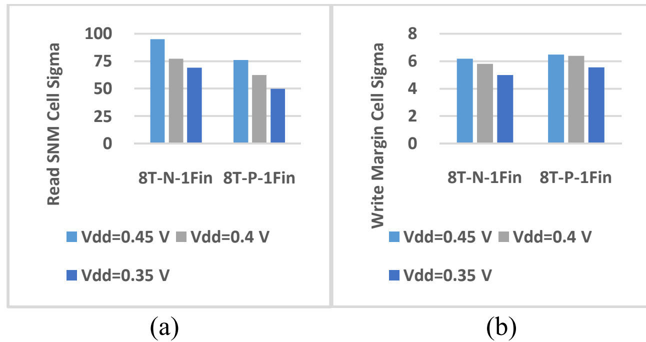


Figure 13. (a) Read SNM and (b) WM cell sigma values for the proposed 8T for supply voltages of 0.45, 0.4 and 0.35 V.

Table 3: Types of the read access transistors for the 8T structures.

Name of structures	Type of read access transistors
8T-N1, 8T-P1	N1
8T-NCUS, 8T-PCUS, 8T-NCUB, 8T-PCUB	N2-1
8T-N3, 8T-P3	N3

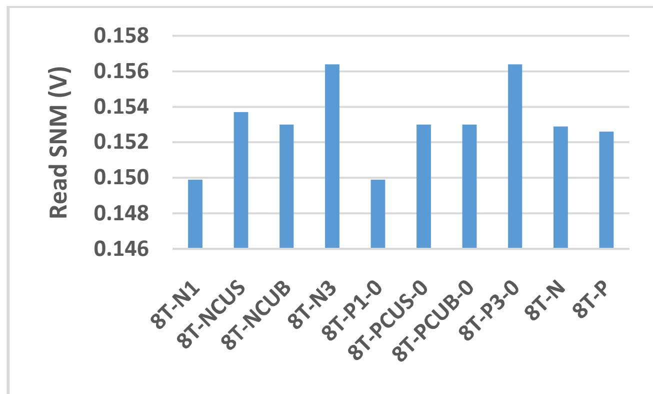


Figure 14. Nominal read SNM for different 8T structures.

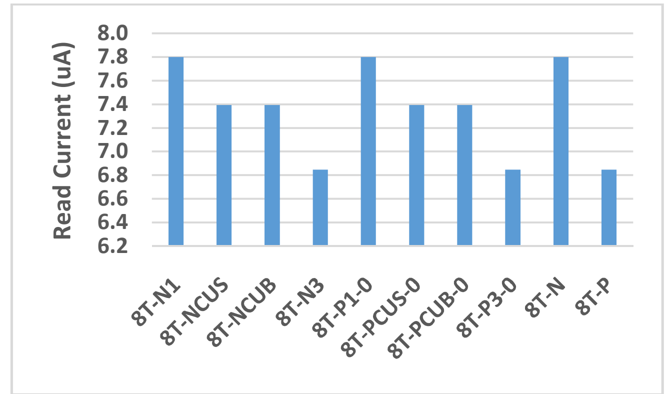


Figure 15. Nominal read current for different 8T structures.

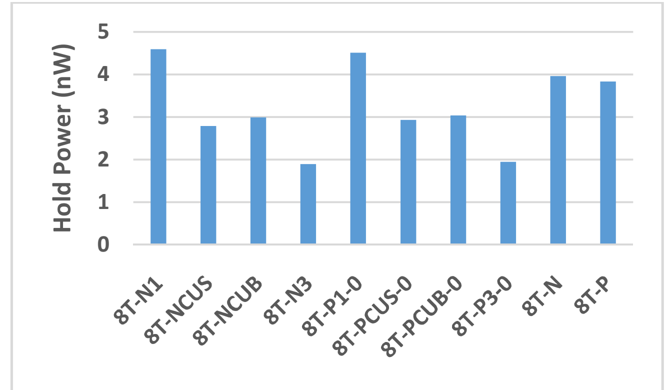


Figure 16. Nominal hold power for different 8T structures.

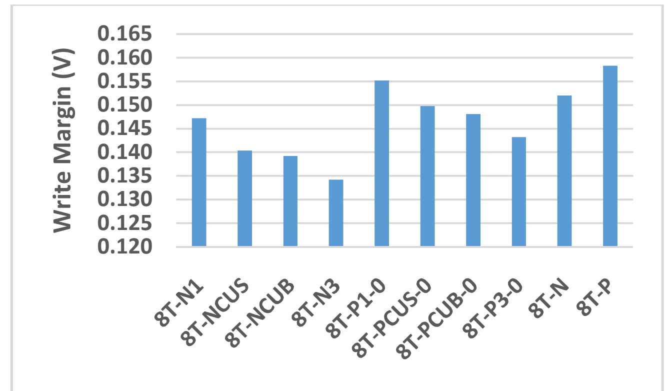
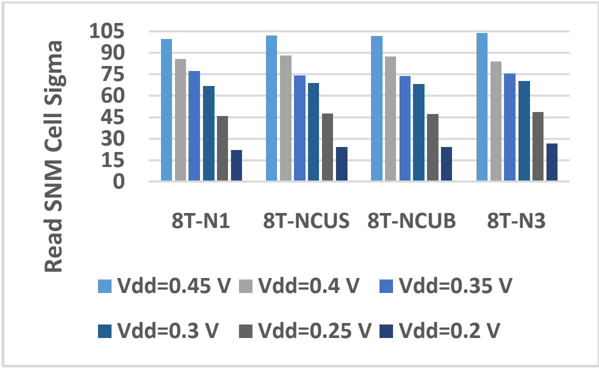
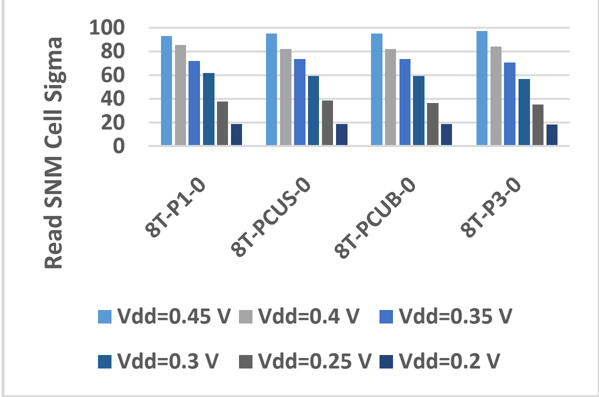


Figure 17. Nominal WM values for different 8T structures.

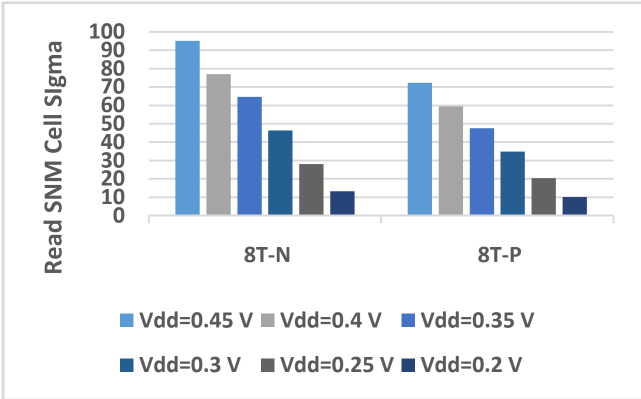
Next we study the effect of the process variation on the read SNM and WM cell sigmas of the ten cells at the supply voltages of 0.45, 0.4, 0.35, 0.3, 0.25, and 0.2V. The read SNM cell sigmas which are shown in Figure 18 reveal that the read SNM cell sigma values of 8T structures including 8T-N and 8T-P are well above six. Figure 19 presents the WM cell sigmas which indicate that the modifications to the 8T-N and 8T-P have improved the stabilities compared to other 8T structures. Also 8T-P has WM cell sigma more than six even at the supply voltage of 0.25 V. This indicates that this cell has a good write stability even in the presence of the process variation.



(a)



(b)

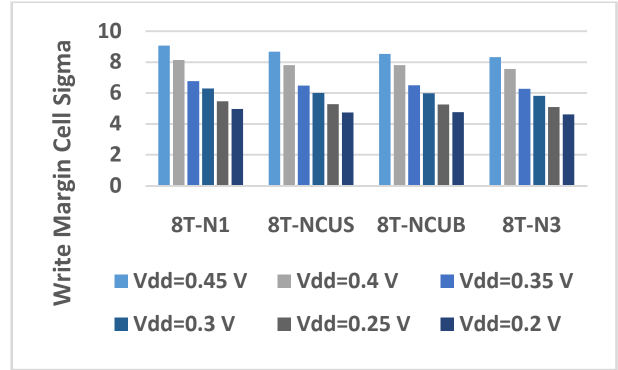


(c)

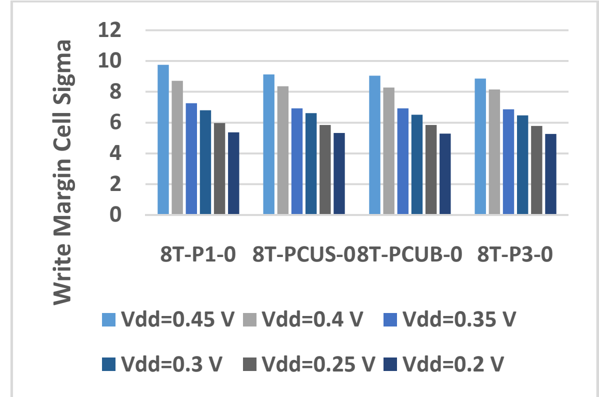
Figure 18. Read SNM cell sigma values for 8T cells (a) with N type write access transistors, (b) with P type write access transistors and (c) 8T-N and 8T-P.

6. Conclusion

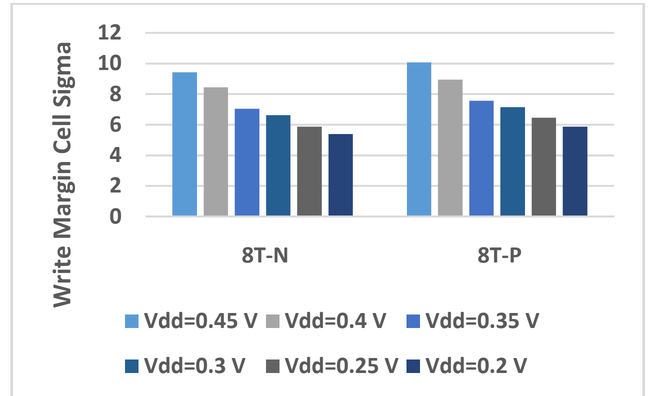
In this paper, the SRAM cell structures based on the 5 nm FinFET technology featuring different underlapped devices were studied. The study included previously proposed 6T-NCUS and 6T-NCUB structures and two cells of 6T-PCUS-0 and 6T-PCUB-0 in this work. These cells made use of asymmetric underlapped transistors. The introduced structures exploited P type access transistors and pre-discharging bitlines to "0" during the read operation. Compared to the structures with N type access transistors, the read current and write margin (WM) were improved while the static power and read SNM were slightly deteriorated using these structures. Furthermore, we studied 8T structures with the 6T cells as the main cores. In order to make the WM larger in these cells which had separated read and write operation paths, less underlap devices were used for the write access transistors. In addition, it was suggested to utilize more underlap for the pull down (pull up) transistors in the structures with the P type access transistors (for the structures with the N type access transistors). Also, it was suggested to double the number of the fins of the write access transistors. These techniques significantly increased the WM and had no adverse effect on the read SNM. For both the 6T and 8T SRAM cells, the impacts of the process variation on the cell characteristics were investigate. It was revealed that the proposed 8T-P structure possessed a WM cell sigma higher than six even for the supply voltages as low as 0.25 V.



(a)



(b)



(c)

Figure 19. WM cell sigma values for 8T cells (a) with N type write access transistors, (b) with P type write access transistors and (c) 8T-N and 8T-P.

6. References

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