An Efficient Semi-Analytical Current Source Model for FinFET Devices in Near/Sub-Threshold Regime Considering Multiple Input Switching and Stack Effect

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Abstract

Nanoscale FinFET devices are emerging as the transistor of choice in 32nm CMOS technologies and beyond. This is due to their more effective channel control, higher ON/OFF current ratios, and lower energy consumption. This paper presents an efficient current source model (CSM) for FinFET devices operating in the near/sub-threshold regime, considering multiple input switching (MIS) and accounting for the effect of internal node voltages of the logic cell. The main problem of the traditional MIS model is that it requires high-dimensional lookup tables. In this paper, we combine non-linear analytical models and low-dimensional CSM lookup tables to simultaneously achieve high modeling accuracy and time/space efficiency. The proposed framework is verified by experimental results on the 32nm Predictive Technology Model for FinFET devices.

Keywords

Current source model (CSM), FinFET, multiple input switching (MIS), stack effect

1. Introduction

With the dramatic downscaling of layout geometries, the traditional bulk CMOS technology is facing significant challenges due to several reasons such as the increasing leakage and short-channel effects (SCEs) [1]. FinFET devices, a special kind of quasi-planar double gate (DG) devices, have been proposed as an alternative for the bulk CMOS when technology scales beyond the 32nm technology node [2][3]. It has been proved in [4] that FinFET devices outperform bulk CMOS devices in ultra-low power designs by allowing for higher voltage scalability. Another unique feature of FinFET devices is the *independent gate control*, i.e., the front gate and the back gate can be controlled by separate signals, which enables more flexible circuit designs [6]. Due to the capacitor coupling of the front gate and the back gate, the threshold voltage of the front-gate-controlled FET varies in response to the back gate biasing, and vice versa. Previous work [5] utilized the independent gate control for FinFETs in the pull-down network of an SRAM cell to keep the ~20 pA/μm standby power budget, whereas the authors of [6][7] studied joint gate sizing and negative biasing on the back gate of FinFET devices and demonstrated significant power reduction.

Our main goal in this work is to design an accurate timing analysis model that accounts for multiple input switching and stack effect, taking into account the afore-mentioned features of FinFET devices. *Static timing analysis* (STA) is a well-known method to verify the circuit timing and considerable efforts have been invested in developing voltage-based statistical gate delay models [8]. However, their accuracy is limited as the input and output voltage dependencies are approximated using input slew and output load. The accuracy degradation would be more severe for FinFET devices operating in the near/sub-threshold regime as the crosstalk noise more significantly impacts the signal integrity of such devices [9].

Current source-based logic cell modeling (CSM) has been introduced as an alternative approach for timing calculation and verification [10]~[14] in order to address key shortcomings of conventional voltage-based timing analysis methods. Instead of recording the delays and output slews in lookup tables (LUTs), CSM builds an equivalent circuit model for each logic gate using independent current sources and several equivalent capacitances. The values of current sources and capacitances are pre-characterized and recorded in *standard CSM LUTs*, where the terminal voltages are used as the index keys. The output waveforms are calculated in a discrete-time manner using pre-characterized LUTs based on given input waveforms. In presence of the input noise, the CSM method achieves very high accuracy in producing output waveforms and calculating delays, because the current and capacitances at various combinations of input and output voltages are all pre-characterized. In addition, CSM is much faster compared to a circuit simulator such as SPICE because the former indexes pre-characterized LUTs to obtain values of currents and capacitances. Finally, the LUT-based approach in CSM can be easily applied to different supply voltage regimes, and thus is very suitable for simulating and analyzing circuits that support burst-mode applications and operate in multiple supply voltage regimes. Thanks to these capabilities, CSMs can be used in timing analysis to effectively reduce errors in delay calculation.

Multiple input switching (MIS) effect is one of the key considerations which determine the model accuracy in CSM. Authors in [15] have provided a complete MCSM (Multiple Input Switching Current Source Modeling) which is not only capable of handling simultaneous input switching but also captures the effect of internal node voltages. Other kinds of MCSM are also presented in [16][17]. However, there are some problems in extending those MCSM models to FinFET devices operating in the near/sub-threshold regime. First, the models used in bulk CMOS logic cells do not consider the variation of threshold voltage of the front-gate-controlled FET in response to the back gate biasing, and vice versa. When the supply voltage drops to the near/sub-threshold voltage regime, the driving current becomes very

sensitive to the variation of threshold voltage. In addition, the above-mentioned MCSM models require very high-dimensional (at least four) lookup tables to account for all the terminal voltages (including the internal node voltage), and the time/space complexity will grow exponentially with the increase of the number of input signals.

To solve these problems, we develop an efficient current source modeling framework in this paper for FinFET devices. The main contributions of this paper are as follows:

1. We develop CSM for FinFET devices operating in the near/sub-threshold regime. The unique feature of independent gate control is also carefully accounted for.
2. We extend our CSM to multiple-input logic cells (e.g., NAND, NOR), accounting for the MIS effect and the stack effect.
3. We use a semi-analytical approach to reduce the time/space complexity while maintaining high modeling accuracy.

The proposed technique determines all the component values in the equivalent circuit model given the applied voltages on the front-gate-controlled and back-gate-controlled FETs, the output voltage, as well as the voltage at the internal nodes for multiple-input logic gates. We use a simple example to illustrate the meaning of the term "semi-analytical". For one component value of interest, e.g., a parasitic capacitance C, we derive an analytical equation relating it to the terminal voltages x, y, u and v. The functional form of this equation is the same for all combinations of terminal voltages. However, the equation also depends on a set of pre-characterized regression coefficients stored in LUTs. Suppose that $C(x,y,u,v) = f\big(\mathbf{A}(x,y,u), \mathbf{B}(x,y,v)\big)$, and coefficients $\mathbf{A}(x,y,u)$, $\mathbf{B}(x,y,v)$ are stored in LUTs corresponding to the (x,y,u) or (x,y,v) pair. This example captures the basic principle of the semi-analytical approach although the actual FinFET CSM considering MIS is more sophisticated. Notice that we only use 3D LUTs in our semi-analytical method to reduce the storage space requirement. Although the characterization process is expensive, it is done only once and the results are stored into compact low-dimensional LUTs.

2. Characteristics of FinFET Devices in Near/Sub-Threshold Regime

2.1. Independent Gate Control for FinFET Devices

FinFET devices show better suppression of the short channel effect, lower energy consumption, higher supply voltage scaling capability, and higher ON/OFF current ratio compared with the bulk CMOS counterparts [3][5]. In addition to better control over the channel by using double gates, the FinFET structure allows for fabrication of separate front and back gates. In this structure, each fin is essentially the parallel connection of the *front-gate-controlled FET* and the *back-gate-controlled FET*, both with width H equal to the height of the fin. A unique feature of FinFET devices is the *independent gate control*, where the front and back gates are tied to different control signals.

Independent gate control makes it possible to apply different voltages to the front and back gates of a single fin, and thereby, allowing for more flexible circuit designs. Due to capacitor coupling of the front gate and the back gate of a FinFET transistor, the threshold voltage of the front-gate-controlled FET varies in response to the back-gate voltage, and vice versa. Under a relatively small back-gate voltage, a linear relationship between the change of the threshold voltage of front-gate and the back-gate voltage is observed (suppose that we consider N-type FETs):

$$\frac{dV_{th}}{dV_{BN}} = -\frac{C_{oxb} \cdot C_{si}}{C_{oxf} \cdot (C_{oxb} + C_{si})} \tag{1}$$

where C_{si}, C_{oxf}, and C_{oxb} are the body capacitance, front-gate capacitance, and back-gate capacitance, respectively; V_{BN} is the voltage level applied to the back gate of the N-type fin. Eqn. (1) shows that decreasing the back-gate voltage of the N-type fin results in the increase of V_{th} of the front-gate-controlled N-type FET and therefore an exponential decrease of the leakage current.

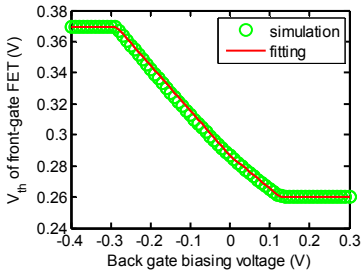

Figure 1. V_{th} of the front-gate-controlled N-type FET v.s. back-gate voltage.

Figure 1 shows the relationship between the threshold voltage of the front-gate-controlled FET and the back-gate voltage from the Hspice simulation. Please note that the threshold voltage will not further decrease (or increase) when we increase the back-gate voltage higher than a specific value $V_{BN,max}$ or lower than a specific voltage level $V_{BN,min}$.

We use a piecewise linear function to represent the impact of the back-gate voltage V_{BN} on the change of the threshold voltage $\Delta V_{th}(V_{BN})$:

$$\Delta V_{th}(V_{BN}) = \begin{cases} \Delta V_{th,max}, & V_{BN} < V_{BN,min} \\ k_1 V_{BN}, & V_{BN,min} \le V_{BN} < 0 \\ k_2 V_{BN}, & 0 \le V_{BN} < V_{BN,max} \\ \Delta V_{th,min}, & V_{BN} \ge V_{BN,max} \end{cases} \tag{2}$$

There are four fitting parameters in the above equation: $k_1, k_2, V_{BN,min}, V_{BN,max}$. k_1 and k_2 represent the $\frac{dV_{th}}{dV_{BN}}$ values in Eqn. (1) when $V_{BN} < 0$ and $V_{BN} > 0$, respectively, and are both less than 0. Notice that k_1 and k_2 are not exactly equal to each other in general, which means that the capacitances C_{si}, C_{oxf}, and C_{oxb} are not exactly the same when $V_{BN} < 0$ (reverse back-gate biasing) and $V_{BN} > 0$ (forward back-gate biasing.) Similarly, $\Delta V_{th}(V_{FN})$ is the threshold voltage change of the back-gate-controlled FET as a function of the front-gate voltage V_{FN}, which also satisfies Eqn. (2). In our experiment, we have the fitting results (k_1, k_2, $V_{BN,min}$, $V_{BN,max}$) = (-0.2897, -0.2098, -0.29V, 0.12V). The threshold voltage of the front-gate-controlled FET accounting for the effect of the back-gate voltage is then given by

$$V_{th,F} = V_{th0} + \Delta V_{th}(V_{BN}) \quad (3)$$

Similarly, the threshold voltage of the back-gate-controlled FET is given by $V_{th,B} = V_{th0} + \Delta V_{th}(V_{FN})$. Please note that the V_{th0} value is the same for both front-gate-controlled and back-gate-controlled FETs because they share the same fin. Experimental results show that the average and maximal fitting errors are 0.3% and 0.94%, respectively.

Authors in [5][6][7] proposed and applied different implementation modes of FinFET logic gates to exploit the unique feature of independent gate control. For the N-type or P-type fin, there are two different connection modes: (i) the double gate (DG) mode, where the front gate and the back gate of the fin are tied together to the input signal, and (ii) the independent gate (IG) mode, where one of the gate is driven by the input signal and the other is connected to a pre-defined biasing voltage or to the ground. For multiple-input logic cells (e.g., NAND, NOR), there is another IG mode connection where the front gate and back gate are driven by different input signals. These different modes achieve a trade-off between power consumption and rise/fall delay. We illustrate in Figure 2 three examples of implementations of an NAND gate. In Figure 2 (a), we use the double gate mode for both the N-type and P-type fins. In Figure 2 (b), we use the independent gate mode for both N-type and the P-type fin, where each back gate is tied to a certain biasing voltage to control the threshold voltage of the front gate. In figure 2 (c), we use double gate mode for N-type fin while the two gates of the P-type fin are driven by different input signals.

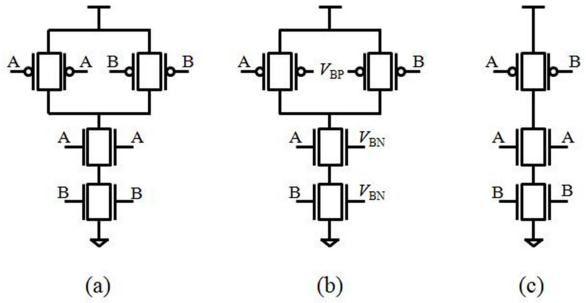

Figure 2. Different FinFET-based NAND gate designs

2.2. Semi-Analytical Modeling of Driving Currents for FinFET Devices in the Near/Sub-Threshold Regime

The driving current is a critical parameter in FinFET modeling. In order to build an equivalent current source model for FinFET devices, we aim at accurate and efficient modeling of the driving current of each fin by combining non-linear analytical models and low-dimensional lookup tables. Taking the N-type fin as an example, in the near/sub-threshold regime, the driving current I_{FN} (I_{BN}) for the front(back)-gate-controlled FET is a function of gate drive voltage V_{FN} (V_{BN}) and the drain-to-source voltage V_{ds}. Considering that each fin is essentially a parallel connection of the front-gate-controlled FET and the back-gate-controlled FET, I_N is the sum of the driving current of the front gate and that of the back gate, i.e., the total driving current of the fin, and is given by:

$$I_N = I_{FN} + I_{BN}. \quad (4)$$

Obviously, I_N depends on V_{FN}, V_{BN} and V_{ds} values. Our goal is to use no larger than 2-D lookup tables to determine the driving current I_N (or I_P) under these three applied voltage levels V_{FN} , V_{BN} and V_{ds} , accounting for the effect of threshold voltage change. Please note that this modeling is general in that it can be applied to N-type fins with both DG and IG connection modes as shown in Figure 2.

We use a semi-analytical model to fit I_{FN} with respect to V_{FN}, V_{BN} and V_{ds} based on the transregional model provided in [18] in the near/sub-threshold regime using the following form:

$$I_{FN}(V_{FN}, V_{BN}, V_{ds}) = \mathbf{C}(V_{FN}, V_{ds}) \cdot e^{\mathbf{A}(V_{FN},V_{ds}) \cdot V_{th,F}^2 + \mathbf{B}(V_{FN},V_{ds}) \cdot V_{th,F}}, \quad (5)$$

where $\mathbf{A}(V_{FN}, V_{ds})$, $\mathbf{B}(V_{FN}, V_{ds})$, and $\mathbf{C}(V_{FN}, V_{ds})$ are fitting parameters. The dependencies of the driving current on V_{FN} and V_{ds} in the transregional model are absorbed into these fitting parameters. The value $V_{th,F}$ depends on $\Delta V_{th}(V_{BN})$, as shown in Eqn. (3). Notice that the front gate and the back gate have a symmetric structure. Hence, the same fitting parameters can be used to calculate the current of the back gate:

$$I_{BN}(V_{FN}, V_{BN}, V_{ds}) = \mathbf{C}(V_{BN}, V_{ds}) \cdot e^{\mathbf{A}(V_{BN},V_{ds}) \cdot V_{th,B}^2 + \mathbf{B}(V_{BN},V_{ds}) \cdot V_{th,B}} \quad (6)$$

The above method combines the non-linear analytical models and small-size lookup tables, and simultaneously achieves high modeling accuracy and space/time efficiency. Compared with the transregional model in [18], the lookup table-based model in Eqns. (5) and (6) results in much higher accuracy because some parameters in the exponential model or the transregional model [18], such as the subthreshold slope n , which depends on V_{FN} and V_{ds} [19]. Our experimental results show that the lookup table-based model achieves an average error of 0.81%, compared with that of 4.23% from the transregional model. Similarly, the proposed method can be applied to the P-type fin to determine the corresponding driving current I_P.

3. Conventional Current Source Model Considering Multiple Input Switching

The idea of current source-based modeling of logic cells was introduced about a decade ago with the goal of more accurately capturing the dependency of logic cell's timing behaviors on its input and output voltages. The CSM method builds an equivalent circuit model for each logic gate using independent current sources and several equivalent capacitances. The MCSM provided in [15] considers multiple input switching (MIS) and accounts for the effect of internal node voltages. We make an enhancement from that model and show an example of our MCSM (which we refer to as the Complete MCSM) of a two-input FinFET NAND gate. From our experimental results, we found that the miller

effect between input nodes and internal nodes is more significant for FinFET cells operating in the near/sub-threshold regime, because of the increased stacking effect. In order to account for this effect, we add two miller capacitances to the original MCSM. This model can accurately capture simultaneous switching of multiple input signals while accounting for the internal node voltages of the logic cell.

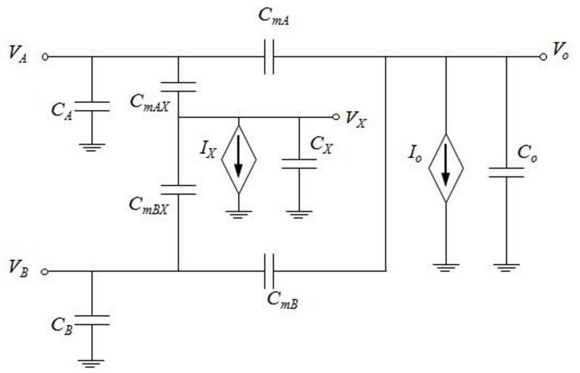

Figure 3. A complete MCSM of a FinFET two-input NAND gate

In general, the CSM-based timing analysis is comprised of two phases: the characterization phase and the evaluation phase. In Figure 3, V_A and V_B are the input voltage levels and V_o is the output voltage level of the NAND gate. In the characterization phase, an equivalent circuit model for each logic cell in the standard cell library is proposed and accurate circuit simulators (e.g., SPICE) are used to obtain the component values in the equivalent circuit model at different input and output voltages. If the stack effect is considered, the voltage of the internal node V_X should also be included. Each component in Figure 3 is expressed as a function of V_A, V_B, V_o and V_X. C_A, C_B, C_o and C_X denote the equivalent capacitances at the two inputs, the output and the internal nodes of the NAND gates, respectively. C_{mA} and C_{mB} denote the Miller capacitances between input and output nodes, while C_{mAX} and C_{mBX} denote the Miller capacitances between input and internal nodes. These capacitance values are characterized through a series of SPICE-based transient simulations, in which saturated ramp input and output voltages are applied to input and/or output and internal nodes while the output current is monitored. The values of current sources I_o and I_X in response to DC voltage levels on the inputs, output and internal node are also determined based on DC simulations. Multiple 4D LUTs are generated to store the above component values at different (V_A, V_B, V_o, V_X) combinations.

In the evaluation phase, we calculate the waveform of both the output and the internal nodes using pre-characterized driving currents and equivalent capacitances, as well as sample values of the input voltages. The accuracy of the CSM method depends on both the LUT precision, i.e., the resolution of the voltage levels V_A, V_B, V_o and V_X in the LUT, and the sampling frequency of the input waveform.

The original MCSM (ignoring the miller effect between input nodes and internal node) has been proven to provide high accuracy [15], and there is no doubt that our model illustrated in Figure 3 will be able to generate even more accurate results, by taking into consideration more complex effects. However, the main problem of this model is that it requires a large memory space to store the 4D LUTs corresponding to all the driving currents and the parasitic capacitances. What is more, the complete MCSM has an exponential complexity of LUTs, i.e., as the number of internal nodes increases, the number of LUT dimensions increase which in turn results in exponential increase in time and space complexity of timing tools. In the next section, we present an efficient alternative model that can achieve almost the same level of accuracy but the space complexity is reduced a lot.

4. Efficient MCSM for FinFET Devices

To extend the CSM-based method to FinFET devices operating in near/sub-threshold voltage regimes, we should develop a model that can appropriately account for the fact that the threshold voltage of the front-gate-controlled FET is affected by the back-gate voltage, and vice versa. In addition, to solve the above-mentioned space complexity problem while maintaining high modeling accuracy, we propose an efficient way to construct a semi-analytical MCSM for the FinFET logic cells in this section based on the physical relations of the current and gate voltages and observations from our experimental data. Instead of storing the model component values at all the different (V_A, V_B, V_o, V_X) combinations, we use at most 3D LUTs to reduce the storage space requirement. In Section 4.1, we analyze the modeling of current sources I_o and I_X with respect to the voltage levels at different nodes. A combined analytical and LUT based model is provided to reduce the space complexity to 2-dimentional. Section 4.2 focuses on the compressed modeling of input and miller capacitances, and Section 4.3 deals with the parasitic capacitances at the output and internal nodes using the method of separating variables (SVM). Finally, the CSM LUT construction process is summarized in Section 4.4.

Please note that because of the increasing stack effect in FinFET devices, FinFET standard cells are restricted to three or even two inputs. In this paper, we use a FinFET two-input NAND gate as an example to describe our efficient MCSM. The semi-analytical modeling framework can be easily extended to the other types of FinFET gates, such as 2-input NOR gates and 3-input gates. The generalization process will be similar and is not discussed in detail in this paper due to space limitation.

4.1. Modeling of Driving Currents

We have modeled the driving currents as two current sources in the MCSM provided in Figure 3, and the value of each current source is determined in response to DC voltage levels on the inputs, output and internal node. The simple approach to store the current source values at different (V_A, V_B, V_o, V_X) combinations requires 4D LUTs.

However, the space complexity can be reduced based on the actual components of the current sources I_o and I_X.

Figure 4 shows all the driving current components of a two-input NAND gate. The current components I_{NA} and I_{NB} in this figure correspond to the driving currents of the N-type fins connected to input A and B, respectively, and we can find the similar meanings of I_{PA} and I_{PB}. By comparing the models shown in Figure 3 and Figure 4, we can observe that the current sources I_o and I_X shown in Figure 3 satisfy the following equations:

$$I_o = I_{PA} + I_{PB} + I_{NA}, \quad (7)$$

$$I_X = I_{NB} - I_{NA}. \quad (8)$$

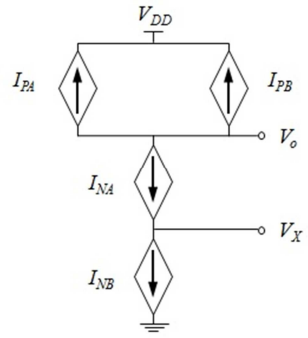

Figure 4. The driving current components of a two-input NAND gate

Notice that although we have different modes of NAND gates in Figure 2, they share the same MCSM structure as well as the driving current components model shown in Figure 4. For DG mode connection in Figure 2 (a) or IG mode connection with pre-defined biasing voltages in Figure 2 (b), each driving current component in Figure 4 is calculated as the total driving current of each fin, i.e., the sum of driving currents from both the front gate and the back gate. For IG mode connection like the P-type fin in Figure 2 (c) where the front gate and back gate are connected to different input signals, I_{PA} should be calculated as the current of the one gate in the P-type FET (which is connected to input A), while I_{PB} is calculated as the current of the other gate of the same fin (which is connected to input B). In this way, we can use a universal model for different modes of FinFET cell structures implementing the same logic.

As discussed in Section 2, each current component in Figure 4 can be characterized using a semi-analytical approach with 2D LUTs. The independent gate control effect is accounted for in this method by deriving the analytical formula of threshold voltage change. Hence, we are able to characterize and store all the required parameters using **the same set** of 2D lookup tables for different modes of FinFET cell structures implementing the same NAND logic.

4.2. Modeling of Input and Miller Capacitances

The LUTs corresponding to input capacitances (e.g. C_A) and miller capacitances (e.g. C_{mA}) can be compressed based on the physical connection. Taking C_{mA} as an example, from Figure 3, we can observe that it has almost no physical connection with input B, so the value of C_{mA} has very little dependency on the voltage level of V_B. As a result, we can simply store the value of C_{mA} at different (V_A, V_o, V_X) combinations, which results in 3D LUTs. The similar approach can be performed for other input or miller capacitances and experimental results show that the accuracy is almost not affected from our method of compression (i.e., dimension reduction.)

4.3. Modeling of Output and Internal Node Capacitances

Based on our observation, the capacitances at output or internal node have strong dependencies on all the voltage levels of V_A, V_B, V_o and V_X. So the LUTs corresponding to these capacitances cannot be compressed in a straightforward way. However, the *SVM* can be used to model each component using a linear combination of several components, each of which only depends on a subset of the node voltage levels. Taking C_o as an example, Figure 5 shows the value of the capacitance as a function of V_A under different V_B values when $V_o = 0.2\text{V}$ and $V_X = 0.1\text{V}$.

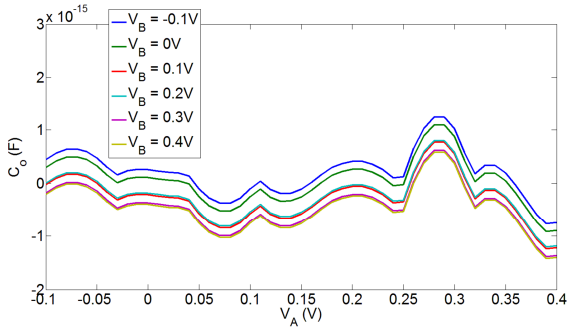

Figure 5. The relationship between C_o and V_A under different V_B values at $V_o = 0.2\text{V}$ and $V_X = 0.1\text{V}$

It can be observed from Figure 5 that at a certain (V_X, V_o) pair, the difference between C_o values at two V_B levels is constant regardless of the voltage level V_A. Using the method of separating variables, we can model C_o as a sum of two voltage-dependent components a_o and b_o: the first one is independent of V_B whereas the latter one is independent of V_A, as shown in Eqn. (9):

$$C_o = a_o(V_A, V_X, V_o) + b_o(V_B, V_X, V_o). \quad (9)$$

Similar approach can be applied to the capacitance at the internal node:

$$C_X = a_X(V_A, V_X, V_o) + b_X(V_B, V_X, V_o). \quad (10)$$

In this way, we need only 3D LUTs to store the corresponding parameters and the storage overhead is significantly reduced.

4.4. Efficient MCSM LUT Construction

After studying the modeling of driving current and the parasitic capacitances, our proposed efficient MCSM LUT construction process can be concluded as follows: in the characterization phase, we perform characterization as well as curve fitting and SVM as mentioned earlier and record the coefficient parameters into the LUTs with index of voltage levels of interest. In the evaluation phase, we use the

coefficient and LUTs to calculate the current and capacitance values such as I_o, I_X, C_o, and C_X, under the index voltage combinations. Since the analytical calculation requires constant time, the speed of simulation will be very fast. The calculated current and capacitance values can be used to derive the exact output waveform given the voltage waveforms at different input nodes.

The proposed efficient semi-analytical MCSM method enables accurate current-based timing analysis for FinFET devices. Compared with the conventional complete MCSMs, the space complexity is greatly reduced because we are using lower dimension LUTs for parameter storage.

5. Experimental Results

In this section, we evaluate the accuracy of the proposed efficient semi-analytical MCSM for FinFET devices in calculating the output waveform and delay. We adopt 32nm Predictive Technology Model for FinFET devices, in which the typical threshold voltages of the transistors are around ±0.3V. We set the supply voltage to 0.3V so that the circuits are operated in the near/sub-threshold regime. To ensure that voltage characterization covers the range of the noise, we sweep the input and output voltage from -100 mV to +400 mV with the interval of 10 mV. The characterization is based on HSPICE, and the entire process for FinFET modeling and output waveform calculating takes around 6 hours on a Debian 7 machine with 16 Intel E7-8837 2.66 GHz CPUs and 64 GB memory.

In order to determine the accuracy of the proposed method, we set the conventional complete MCSM as the baseline and compare our work with it in determining the output waveforms. The proposed method and baseline method are compared to the golden results generated using the HSPICE considering multiple input switching and also input noises. We first verify the accuracy of the semi-analytical MCSM in calculating the driving currents and parasitic capacitances at different combinations of node voltages. After that, we demonstrate the accuracy of proposed MCSM in calculating the real output waveforms under noisy inputs.

5.1. Error Analysis of MCSM Parameters

In order to guarantee our model accuracy at every corner of voltage nodes, we use our efficient 2D or 3D LUTs as well as the proposed semi-analytical method to generate driving current and parasitic capacitance values in the MCSM at all different (V_A, V_B, V_o, V_X) combinations. The generated result is then compared with the corresponding value which comes from conventional complete 4D LUTs. The error analysis is shown in Table 1.

Table 1: Proposed model error analysis of a FinFET DG mode two-input NAND gate.

MCSM Parameter	Mean Error	Max Error	MCSM Parameter	Mean Error	Max Error
I_o	<0.01%	<0.01%	I_X	<0.01%	<0.01%
C_{mA}	<0.01%	<0.01%	C_{mB}	0.01%	1.62%
C_{mAX}	<0.01%	<0.01%	C_{mBX}	0.01%	1.63%
C_o	<0.01%	0.02%	C_X	<0.01%	0.02%

It can be observed from Table 1 that our proposed method achieves very good fitting quality. Most of the MCSM parameters can be modeled with an average error less than 0.01%. Notice that data in the above table comes from a DG mode two-input NAND gate in Figure 2 (a). We got the similar result from IG mode NAND gates, except for the I_o value of the IG mode NAND gate in Figure 2 (c), which results in a mean error of 0.3% and a maximal error of 0.74%. The reason is that the P-type FET is connected to different inputs so that the currents I_{PA} and I_{PB} need non-linear curving fitting, as is presented in Section 2.2. But even considering the most sophisticated case, our proposed model is still very accurate at every corner of voltage nodes.

5.2. Output Waveform under Noisy Inputs

To test the accuracy of our model in practice, we use both the complete LUTs and our efficient LUTs to calculate the output waveforms based on the proposed semi-analytical method. We show the DG-mode NAND gate as an example to calculate output waveforms and compare them with the waveforms obtained using HSPICE simulation, considering multiple input switching and also input noises. Figure 6 and Figure 7 show the waveforms of the output node as well as the internal node using different simulators. It can be observed that like the conventional complete LUTs, our efficient LUTs can also provide close-to-spice results. The waveforms generated using our LUTs are almost exactly the same as that are simulated using Hspice.

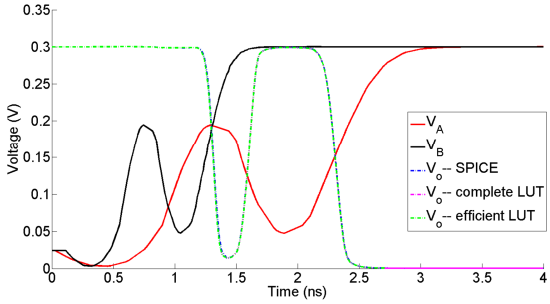

Figure 6. Waveforms of the output node for a two-input NAND using different simulators.

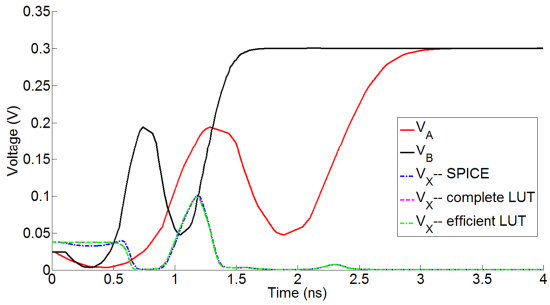

Figure 7. Waveforms of the internal node for a two-input NAND using different simulators.

In timing analysis, the 50%Vdd arrival time is of great interest, and the cell delay definition is based on it. We also make a comparison on the arrival time error between the complete MCSM and our efficient MCSM. The result is shown in Table 2.

Table 2: The arrival time error comparison between complete MCSM and our efficient MCSM

	Point 1	Point 2	Point 3
Complete MCSM	0.192%	0.189%	0.097%
Efficient MCSM	0.193%	0.189%	0.097%

Form Table 2, one can see that our efficient MCSM provides almost the same level of accuracy compared with conventional complete MCSM. Notice that we are using only 2D or 3D LUTs in our proposed method so the space complexity is much smaller. The high accuracy and low space requirement ensure the capability of performing timing calculation and analysis based on the proposed MCSM method.

6. Conclusion

In this paper, we present an efficient semi-analynical multiple input switching current source model (MCSM) for FinFET devices operating in the near/sub-threshold voltage regime. The driving currents and parasitic capacitances are analyzed based on the physical dependencies on different node voltages. Curve fitting and variable separating steps are performed to relate the driving currents and parasitic capacitances to different node voltage levels, and fitting parameters are stored in low-dimensional lookup tables (LUTs). In circuit timing simulation, we perform a semi-analytical calculation to generate the output waveforms. Experimental results show that our proposed efficient MCSM achieves the same level of accuracy as conventional complete MCSM, while the space complexity is greatly reduced.

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