Analysis and Optimization of Sequential Circuit Elements to Combat Single-Event Timing Upsets

Hamed Abrishami, Safar Hatami, and Massoud Pedram
University of Southern California
Department of Electrical Engineering
{habrisha,shatami,pedram}@usc.edu

Abstract—**This paper presents the analysis and optimization of a flip-flop while considering the effect of energetic particle hits on its setup and hold times. First it is shown that the particle hit tightens the setup and hold timing constraints imposed on the flip-flop. Next it is shown how to size transistors of a clocked master-slave CMOS flip-flop to make it more robust against single-event timing upsets. Experimental results to assess the effectiveness of transistor sizing step are provided and discussed.** [1]

I. INTRODUCTION

As CMOS transistors are scaled down toward sub-micron CMOS technology nodes, circuit reliability cannot be ignored. One of the important reliability concerns in today's VLSI circuits is the incidence of soft errors which occur due to various types of radiations, i.e., high energy neutrons present in terrestrial cosmic radiations or alpha particles which originate from impurities in the packaging materials. When these energetic particles hit a sensitive region in a sequential circuit element (SCE), they generate charges which can be collected by source/drain diffusion nodes, causing a single-event upset (SEU). SEU can thereby alter the logic state of the node resulting in a soft error. Moreover, at the particle hit events which SEU doesn't happen, the setup/hold time characteristic of the sequential circuit elements (i.e., latches and flip-flops) alters. This alteration tightens timing constraints.

Due to technology scaling, the supply voltage and the node capacitance in the VLSI circuit decrease. The resulting quadratic reduction in stored charge is the main reason for increased vulnerability to soft errors in nanometer scale technologies.

In an integrated circuit, both sequential and combinational logics are all susceptible to soft errors. A number of researchers have addressed soft errors on combinational logic and proposed solutions to alleviate their effect as single event transition (SET) [1]. The soft error reliability issue for the SCEs (i.e., latches and flip-flops) has also been investigated. In [2] SEU due to particle hit in latches was investigated, and stack tapering and use of explicit capacitance at the feedback node were proposed as hardening techniques. The authors of [3] showed that by proper sizing, it is possible to create immunity from SETs generated in the combinational logic gates. The proposed technique leverages temporal masking by selectively increasing length of the latching windows of the flip-flops, thereby preventing faulty transients from being registered. Unfortunately, none of these works consider the effect of the particle hit on the timing characterizations of SCEs.

Operating frequencies of more than 1 GHz are common in modern integrated circuits. As the clock period decreases, inaccuracy in setup/hold times caused by corner-based static timing analysis (STA) tools becomes less acceptable. Optimism in setup/hold time calculation can result in circuit failure, while pessimism leads to inferior performance [4]. Therefore, accurate characterization of the setup and hold times of latches and registers is critically important for timing analysis of digital circuits [5].

In this paper we study the effect of the radiation on the master-slave flip-flops during their transition mode (i.e., from a timing viewpoint, the particle hit occurs near the triggering edge of the clock). We show, to the best of our knowledge for the first time, that a flip-flop which has been hardened to the radiation is still susceptible to the radiation in a sense that the particle hit tightens the setup and hold timing constraints imposed on the SCEs in the design causing timing violation. We call this effect, ***Single Event Timing Upset (SETU)***.

The remainder of the paper is organized as follows. Section II provides background on the model which is used to evaluate the effect of the particle hits on the SCE characteristics. It also defines the terminology which will be used in subsequent sections. An analytical model formulation to investigate the effect of the particle hit and the transistor sizing method to combat SETU in master-slave flip-flop are introduced in section III. Section IV reports our simulation results whereas section V concludes the paper.

II. BACKGROUND

This section provides the outline of the soft error model that we use. We first explain the model for a single particle strike. Next, we review the notion for the setup time, hold time, and clock-to-q delay for flip-flops and latches.

A. Technology and Particle Strike Model

All results reported in this paper are obtained by HSPICE [9] simulations using 90nm CMOS technology model [10] with 1.2V for the supply voltage and 0.397V (–0.339V) for nominal threshold voltages of NMOS (PMOS) transistors.

The transient current through a reverse-biased p-n junction because of the charge deposition due to a particle hit at a node in the circuit may be modeled as a current pulse I_{hit} at the site of the particle strike [7] as follows:

$$I_{hit}(t) = \frac{2Q}{\tau\sqrt{\pi}}\sqrt{\frac{t}{\tau}}\exp\left(\frac{-t}{\tau}\right) \qquad (1)$$

where Q is the charge deposited as a result of the particle strike and τ is a technology dependent pulse shaping parameter. The

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authors of [8] calculated τ for 90nm technology using device level 3D simulations and reported it to be 90ps. In this paper we use the same value for τ .

A soft error occurs when the collected charge, *Q,* exceeds some critical charge level, Q_{crit}, of a circuit node. Q_{crit} is the minimum charge injected in order to flip the value of the node. When a particle hits the p-type diffusion area, it generates a current which tries to upset bit 0 stored in the node. If the area is n-type, the current tries to upset the stored bit with value 1.

B. Sequential Circuit Elements

Latches and flip-flops are sequential circuit elements used in synchronous designs where a clock edge is used to sample and store a logic value on a data line. The **setup time,** τ_s, is the *minimum time before* the active edge of the clock that the input data line must be valid for reliable latching. Similarly, the **hold time**, τ_h, represents the *minimum time* that the data input must be held stable *after* the active clock edge. The active clock edge is the transition edge (either low-to-high or high-to-low) at which data transfer/latching occurs. The **clock-to-q** delay (t_{c2q}) refers to the propagation delay from the 50% transition of the active clock edge to the 50% transition of the output, q, of the latch/register.

In general, a STA tool reads in a circuit netlist, a cell library, and a clock period *T* [4]. The tool reports whether new data values can be introduced in a (pipelined) circuit every *T* seconds. This analysis is accomplished by computing the worst **setup slack** (s_s) and the worst **hold slack** (s_h) for any flip-flop in the circuit [6].

If a slack is negative, it is said to be "violated". If a setup slack, s_s, is violated, the circuit can operate correctly only by increasing *T*. If a hold time, s_h, is negative, the circuit will not function correctly unless delay elements are inserted on the short paths in the combinational logic.

III. CIRCUIT LEVEL ANALYSIS

We describe a selective transistor-level sizing approach for a master-slave flip-flop (MSFF). In this technique, we first study the circuit of the flip-flop which we want to make robust to the particle hit. Then we introduce an analytical model for characterizing the effect of a particle hit which causes SETU for a conventional master-slave flip-flop. This analysis is performed to provide insight into how to do the transistor-level sizing to have the best alleviation of the SETU. Although not discussed in this paper, similar analysis and optimization steps can be applied to other types of flip-flops.

A. Analytical Model

A negative-edge triggered FF is shown in Figure 1. This MS flip-flop, which is quite common in ASIC designs, consists of a positive and a negative latch in series. We consider the particle hit in the master latch since the setup and hold times of the flip-flop are dependent on the transistor sizes of this latch. Through analysis and simulations of the master latch of the FF depicted in Figure 1, we know that *Qbar* is the node which is sensitive to the particle hit. We show our analysis for this node (the analysis for *Q* is similar). Without loss of generality, suppose the input to the latch is 1, i.e., *Qbar* and *Q* values are 0 and 1, respectively. An energetic particle hits the p-diffusion area at *Qbar* and creates a positive current which increases the voltage level of the node. The hit occurs at time t_{hit}, which is before the triggering edge of the clock. The analysis for the case in which the value of *Qbar* is 1 and a particle hits the n-diffusion area at *Qbar* is similar and omitted for brevity.

Figure 2 shows the current-based model of the positive latch. The topology of the circuit changes by the triggering edge of the clock, i.e., when the clock signal is high the input clocked-inverter passes the input and the feedback loop is open (feedback clocked-inverter is OFF); the opposite is true when clock signal is low. By writing a KCL equation at node Qbar, using equation (1) and CMOS current equation, V_{Qbar} before the negative edge of the clock is given by:

$$V_{Qbar}(t_{clkedge}) = \frac{1}{C_{Qbar}} \int_{t_{hit}}^{t_{clkedge}} \left(\begin{array}{l} \frac{2Q}{\tau\sqrt{\pi}} \sqrt{\frac{t}{\tau}} \exp\left(\frac{-t}{\tau}\right) \\ + \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(2(V_{GS} - V_{th}) V_{Qbar} - V_{Qbar}^2\right) \end{array} \right) dt \qquad (2)$$

Where C_{Qbar} is the capacitance at node *Qbar* and $t_{clkedge}$ is time instance at which the falling edge of the clock arrives (latching action) and t_{hit} is the time instance for particle hit at *Qbar*. The pull-down network of the input clocked-inverter, modeled as an equivalent NMOS transistor, operates in the linear region (Schichman-Hodges current equation).

As mentioned in II.A, τ = 90ps for the 90nm CMOS technology and *Q* is the amount of charge deposited by the particle hit in (1).

By applying the derivative operator on both sides of (2) and considering that the initial voltage at node *Qbar* is 0, the voltage V_{Qbar} at time $t_{clkedge}$ is calculated easily by a numerical method such as the Euler method. V_{Qbar} at time $t_{clkedge}$ is a function of $t_{skew} = (t_{clkedge} - t_{hit})$.

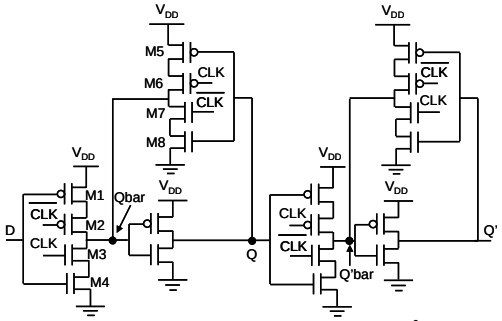

Figure 1. Schematic of a negative-edge triggered C²MOS FF.

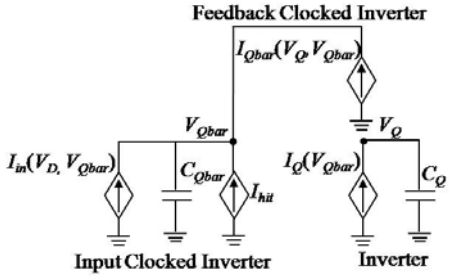

Figure 2. Current based model of a latch

Again by considering the KCL at node *Qbar*, V_{Qbar} after triggering edge of the clock is given by:

$$V_{Qbar}(t) = V_{Qbar}(t_{clkedge}) + \frac{1}{C_{Qbar}} \int_{t_{clkedge}}^{t} \left(I_{hit} + I_{Qbar}(V_Q, V_{Qbar}) \right) dt \qquad (3)$$

where I_{Qbar} is the discharging current of the pull-down network of the clocked-inverter in the feedback path.

To see the evolution of V_{Qbar} after the clock edge (solving equation (3)), we need to consider following two different scenarios. The first case is when a failure (SEU) occurs at the latch output while the other case is when there is no failure at the output of the latch. Since this paper focus is on the timing impacts of the particle hit, i.e., the changes in the setup and hold times of the FF (with no functional value upsets), we shall only consider the second case, i.e., where no SEU happens. The SEU case has extensively been discussed in [11].

We also point out that the probability of SETU is much higher than the SEU probability, to be exact, even particle hits with induced charges smaller than Q_{crit} can cause rather large variation in timing characteristics of the FFs.

1) Non-failure Scenario

In this case, V_{Qbar} does not flip and keeps its original value (here 0), this means no SEU happens. Similarly, the output voltage of the latch (V_Q) does not change. Since V_{Qbar} does not reach the threshold point ($V_{DD}/2$) for V_Q to flip from 1 to 0, the pull-down network of the clocked-inverter in the feedback path stays ON and tries to discharge the current which injected to the stricken node. Meanwhile, there is no current passing through the pull-up network which means the transistors in that path are OFF.

By using equation (3) and knowing the voltage of node *Qbar* at the clock edge, we can evaluate that how much the setup time and hold times of the FF change due to the particle hit. The purpose of presenting the above analysis is to show that the problem can be analytically set up and solved; the formulation also gives us insight about what the effect of various transistor sizes are on the timing characteristics of the flip-flop under particle strike condition.

IV. Simulation Results and Discussion

In his section, we first present results to quantify the impact of a particle hit on the setup and hold times of a MSFF. Next we show the sensitivity of SETU to the sizing of each transistor in the discharging path of the input and feedback clocked-inverters. Finally we present a transistor sizing solution to overcome SETU problem in MSFF, resulting in the design of a SETU-retardant MSFF. As a practical solution, to minimize the timing impact of soft particle hits, one must replace the FFs that lie in the critical timing paths from circuit inputs to outputs with the SETU-retardant FF's designed by our sizing procedure.

A. SETU Dependency on Hitting Time and Q

In this section, we investigate the dependency of SETU on t_{hit} as well as the amount of charge (Q) that it deposits in the stricken node. Evidently when Q increases the setup and hold times of the MSFF increase (since hold time for this flip-flop is negative, the increase in hold time means that the absolute value of the hold time decreases). To do this analysis precisely, we define $t_{skew}=t_{clkedge} - t_{hit}$, and with the aid of HSPICE simulation, we show the variation of setup and hold times as a function of t_{skew} and Q. Figure 3 shows the dependency of setup and hold times on t_{skew} for different Q values. It can be seen that, generally speaking, the setup time increases and the absolute value of the hold time decreases with decreasing t_{skew} and increasing Q.

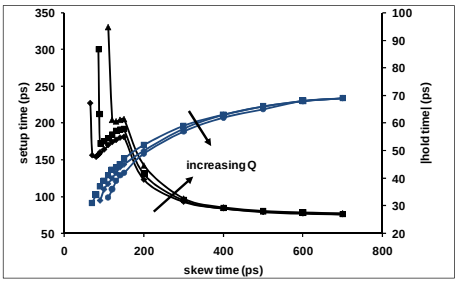

Figure 3. Setup and hold times dependency on tskew and Q

There is, however, a small skew time window in which the setup time decreases when t_{skew} decreases. To explain this phenomenon accurately, we consider three different timing zones for the particle hit as shown in Figure 4 and described next. Notice that, for this analysis and reported simulation results, the D input of the MSFF changes from 1 to 0, which means that *Qbar* is initially 0 and changes to 1 after the triggering (negative) edge of the clock.

I. Skew time zone (1) where $t_{skew}>t_2$

In this time zone, clock signal is high which means that M2 and M3 are ON. The (ON or OFF) state of M1 and M4 is dependent on the data value, D. In our case, since input is high at first, M1 (M4) is OFF (ON). Therefore, *Qbar* is grounded and when particle strikes the n-diffusion area of *Qbar* node, its value becomes negative. Hence, setup time increases (there must be higher stable time for the data to be correctly latched on the triggering edge of the clock).

II. Skew time zone (2) where $t_2<t_{skew}<t_1$

In this time zone, the input changes from high to low, which means M1 goes from the OFF state to the ON state (M4 goes from ON to OFF). Meanwhile, the clock is still high. So, the pull-up network of the input clocked-inverter is ON and forces the voltage level of node *Qbar* to go high. In contrast, the particle hit works to decrease the voltage level of *Qbar* node. Therefore, there is a fighting situation between the pull-up network and the negative charge deposited by the particle hit in the stricken node. This causes a reduction in the setup time.

III. Skew time zone (3) where $t_{skew}<t_1$

In this time zone, M1 (M4) is already ON (OFF) but the clock is in the transition from high to low. Therefore, M2 and M3 are in the transition from ON to OFF. So, the input clocked-inverter becomes open and there is no connection from input to the *Qbar* node anymore. In this situation *Qbar* is floating and hence it becomes quite susceptible to the particle hit. Hence, setup time increases dramatically and after a very small time window, we will see the onset of SEU (which corresponds to small skew times for which the setup time plot is stopped).

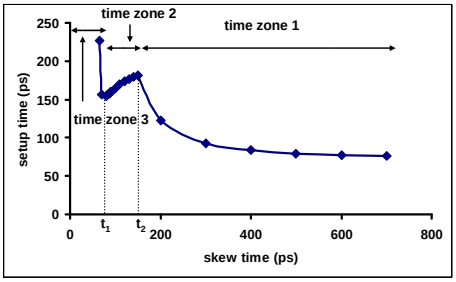

Figure 4. Three different timing zones for particle hit

Table 1 shows the operating regions of the transistors of the input clocked-inverter during these three different skew time zones.

Figure 5 demonstrates the evolution of the voltage level of *Qbar* for different hitting times in different timing zones. We can see that the particle hit in time zone (3) caused a SEU.

Table 1: Operating regions of transistors of input-clocked inverter

Transistor names	Zone (1)	Zone (2)	Zone (3)
M1	OFF	OFF→ ON	ON
M2	ON	ON	ON→ OFF
M3	ON	ON	ON→ OFF
M4	ON	ON→ OFF	OFF

B. Transistor Sizing and Sensitivity Analysis

The change in setup and hold times of the sequential elements due to the particle hit necessitates increasing the size of the transistors to combat the SETU. Since amount of change in timing characteristics of the flip-flop is a function of the precise hitting time of the particle, we have to consider the whole time span of the particle hit during the transition time. We thus need to come up with a sufficient increase in size of selected transistors in SCE to alleviate the SETU effect as much as possible.

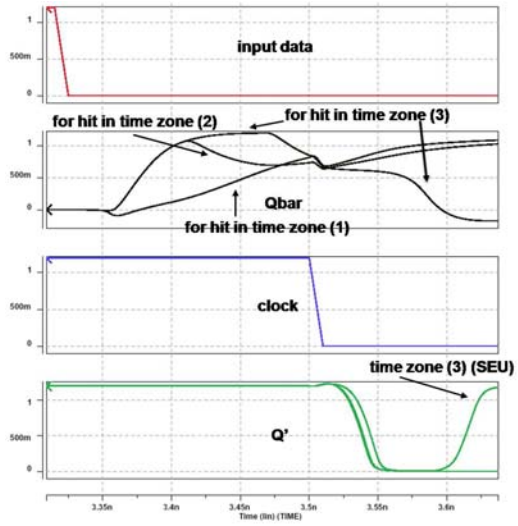

Figure 5. Voltage evolution of Qbar node in different timing zones

As seen from the analytical model of section III.A, in the case of the particle hit at the n-diffusion area (faulty transition at node *Qbar* from 1 to 0) the charging paths in the circuit play a substantial role in the SETU-resilience of the MSFF. Transistor sizing can be performed for different charging paths in the circuit, i.e., charging paths of the input and feedback clocked-inverters. Simulation results show the optimum charging path is the input clocked-inverter. On the other hand, there are two transistors (M1 and M2) in the charging path of the input clocked-inverter. Simulation result shows that increasing the size of M1 by 32% has the same effect as increasing the size of both M1 and M2 each by 16% but the power consumption is higher for the former.

Table 2 shows effect of the selective transistor sizing for different transistors in the charging path of input clocked-inverter. Notice that increasing size of M2 alone does not have any benefit regarding the SETU problem.

To overcome the particle hit at the p-diffusion area (faulty transition at node *Qbar* from 0 to 1), we should increase size of the NMOS transistors to make the pull-down network of the input clocked-inverter stronger. Therefore, we need to take into account both situations of the unwanted transitions from 0 to 1 and 1 to 0. Since the circuit is symmetric, everything which is done for the PMOS transistors should also be repeated for the NMOS transistors to manage the other scenario.

Figure 6 and Figure 7 compare the effect of selective transistor sizing on setup and hold times of MSFF. It is shown that the setup time decreases almost by 15%. We call the properly sized version of the MSFF, SETU-retardant MSFF.

Table 2: Results for the selective transistor sizing for MSFF

Transistor names	Size increase	Area increase	Power consumption increase
Both M1 (M4) and M2 (M3)	16%	6%	2.83%
M1 (M4)	32%	6%	3.27%

V. CONCLUSION

In this paper, we studied the effect of the particle hit at the sequential elements of the logic circuits. We started from the observation that the particle hit tightens the setup and hold timing constraints imposed on SCEs in the design. We showed that the change in the setup and hold times is dependent on the hitting time of the particle and the amount of charge deposited to the stricken node by the hit. Consequently, we introduced and validated an analytical model to size the transistors in the conventional latch to combat the SETU.

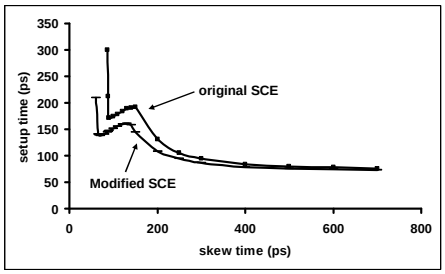

Figure 6. Effect of selective transistor sizing on setup time

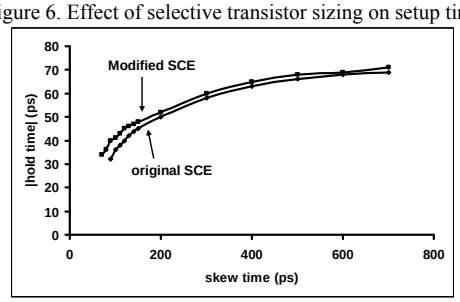

Figure 7. Effect of selective transistor sizing on hold time

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