Statistical Design Optimization of FinFET SRAM Using Back-Gate Voltage

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***Abstract*— In this paper, an optimal approach for the design of 6-T FinFET based SRAM cells is proposed. The approach considers the statistical distributions of gate length and silicon thickness and their corresponding statistical correlations due to process variations. In this method, a back-gate voltage is used as the optimization knob. With the help of Particle Swarm Optimization (PSO), the back-gate voltages that maximize the yield of the SRAM array against read, write, and access time failures are found. It will be shown that with this method a very high yield may be achieved.**

***Index Terms*—SRAM, FinFET, yield, process variations, design for manufacturability, back-gate design.**

I. Introduction

Since SRAM arrays are a major part of the chip area in the state of the art microprocessors [1], their scaling has been a driving for the technology shrinkage. As the device dimensions diminish, the magnitude and effects of parametric variations have been exacerbated. Statistical variability along with scaling of the supply and threshold voltages has degraded the stability of six-transistor (6-T) SRAM cells [2]. In recent years, several statistical schemes have been proposed to maximize the immunity against these variations [3], [4]. For example, the substrate voltage was used in [4] to increase the stability of SRAMs against process variations.

The FinFET [5] transistor structure is one of the attractive options to replace the conventional planar technology due to its improved scalability and gate controllability. In these devices, the gates on either side of the fin can be tied together or electrically isolated to allow an independent biasing scheme. In the tied-gates operating mode the two gates are biased together to switch the FinFET on/off [6]. In the independent-gates operating mode, it is possible to design the device in a way that one gate is used to switch the FinFET on/off and the other one is used to adjust the threshold voltage. This offers dynamic or static performance tunability which gives designers a great flexibility [7]. In [8], authors used this feature to improve the SRAM cell stability. They used two different wordlines that were connected to the front and back gates of each access transistors. In another work, an independent-gate FinFET SRAM has also been successfully manufactured with a considerable leakage reduction [9].

In this work[1], we propose to use the back-gate voltage of FinFET to maximize the yield of the SRAM cell based on these devices against parametric failures. The rest of the paper is organized as follows. Different failure mechanisms in SRAM cells are reviewed in Section II. In Section III, expressions for the read and write stability, read current, and subthreshold power of SRAM cell are presented. The proposed method for the yield optimization will be introduced in Section IV while the results of this method are discussed in Section V. Finally, Section VI concludes the paper.

[1] Preliminary version of this work has been presented in *International Conference on Computer and Communication Engineering,* May 2008, Malaysia.

II. Failure Mechanisms in SRAM Cells

In this section, these failure mechanisms are briefly reviewed.

Read Failure: It occurs due to the corruption of the stored data in the cell while accessing it. During the read operation of the cell shown in Fig. 1 (*VL*= "1" and *VR*= "0"), the voltage at node *R* (*VR*) increases to a positive value, denoted by V_{read}, due to the voltage division between the right access transistor (*AR*) and the right pull down transistor (*NR*). If V_{read} is higher than the trip point of the left inverter (*PL* − *NL*), denoted by V_{trip}, then the cell flips and a read failure occurs.

Write Failure: It is the inability to change the stored data. If the stored data is "1" and we intend to write "0" into it, the node *L* becomes discharged through *BLC* to a lower value. This value is determined by the voltage division between the left PMOS pull up transistor (*PL*) and the left access transistor (*AL*). If *VL* cannot be reduced below the trip point of the right inverter (*PR* − *NR*) then a write failure occurs.

Access Time Failure: It is the inability to produce a predefined voltage difference (*e.g.*, $\Delta\text{min} \approx 0.1V_{dd}$) between the bitlines in the allocated time slot (T_{max}) during the read operation.

III. Modeling of SRAM Failure Metrics

In this section, we present accurate yet simple models for efficiently estimating the failure metrics of the SRAM FinFET. These models are used in the yield optimization in the presence of the process variations. Since our optimization may affect the subthreshold power, we also present the model used for estimating the subthreshold power in this section.

In this work, asymmetrical FinFET (n^+/p^+ polysilicon gate for *n*-channel and p^+/n^+ one for *p*-channel transistors) are considered. The nominal values of key device parameters are summarized in Table I. For implementing the proposed scheme, we also assume that all transistors have one fin to achieve a compact layout area.

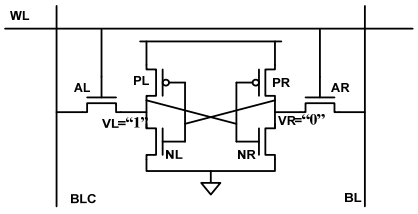


Fig. 1. Schematic of a conventional 6-T SRAM cell.

Table I. Nominal device parameters used for device simulation.

t_{ox} (Oxide Thickness)	1 nm
t_{si} (Silicon Thickness)	10 nm
V_{dd} (Power Supply)	1 V
N_{body} (Channel Doping)	2×10^{16} cm^{-3}
H (Fin Height)	60 nm

A. Threshold Voltage

In the asymmetrical FinFET, the back-gate channel is rarely formed, and hence, for modeling its current, the front threshold voltage (V_{thf}) is sufficient. This threshold voltage can be found using [11]

$$V_{thf} = V_{th\,(4T\text{-}DGMOS)} - rV_{bg}. \quad (1)$$

where V_{bg} is the back-gate voltage, r is the gate-to-gate coupling factor, and

$$V_{th\,(4T\text{-}DGMOS)} = (1+r)\,V_{th\,(3T\text{-}DGMOS)}. \quad (2)$$

The gate-to-gate coupling factor is given by

$$r = \frac{3t_{fox}}{3t_{box} + t_{si}}. \quad (3)$$

where t_{fox} and t_{box} are front and back oxide thicknesses, respectively, and t_{si} is the silicon body thickness. In (2), $V_{th(3T\text{-}DGMOS)}$ can be calculated using [12]

$$\begin{aligned} V_{th(3T\text{-}DGMOS)} &= V_{th\text{-}long\text{-}ch} + \Delta V_{th\text{-}DIBL} + \Delta V_{th\text{-}SCIBL} \\ &= \frac{E_g}{2q} + \phi_B + \frac{(\phi_{Gfs} + \phi_{Gbs}) - (\frac{Q_b}{C_{fox}} - r\frac{Q_b}{2C_{Si}})}{1+r} \\ &\quad - \frac{3t_{Si}t_{fox}V_{ds}}{L_g^2} - \frac{9t_{Si}t_{fox}(E_g/2q)}{L_g^2}. \end{aligned} \quad (4)$$

where E_g is the band gap of the silicon, q is the electric charge, Φ_B is the Fermi potential of the silicon body, Φ_{Gfs} and Φ_{Gbs} are the work function differences between the front-gate and body and the back-gate and body, respectively, Q_b is the depletion charge density of the channel, C_{fox} and C_{Si} are the front gate capacitance per unit area (ε_{si}/t_{fox}) and the body capacitance per unit area (ε_{si}/t_{si}), respectively, L_g is the channel length and V_{ds} is the drain-source voltage. The short channel induced barrier lowering (SCIBL) and drain induced barrier lowering (DIBL) effects are also taken into account. In our device, the thickness of the body is large enough (10nm) for neglecting the quantum effects [12].

B. On-Current

For a good estimation of the *on*-current, the n^{th} power law model [13] is used. The current expressions for the saturation (I_{Dsat}) and linear modes (I_{Dlin}) are given by, respectively,

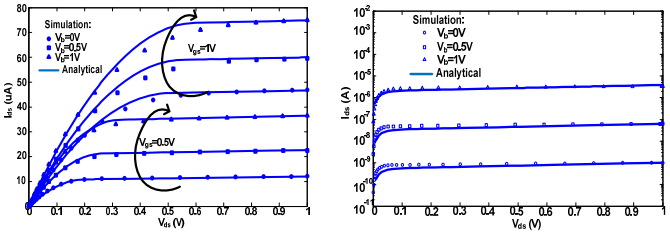
$$I_{Dsat} = \frac{H}{L_g}B(V_{gs} - V_{thf})^n \quad V_{ds} \geq V_{Dsat} \quad (5)$$

$$I_{Dlin} = I_{Dsat}(2 - \frac{V_{ds}}{V_{Dsat}})\frac{V_{ds}}{V_{Dsat}} \quad V_{ds} < V_{Dsat} \quad (6)$$

where H is the fin height and

$$V_{Dsat} = K(V_{gs} - V_{thf})^m. \quad (7)$$

In these equations, m, n, B and K are fitting parameters which are found by fitting the above equations to the results obtained from the device simulations [14]. In the device simulations, the drift-diffusion model along with high field saturation was used for transport. The carrier mobilities were also calibrated using the experimental data for FinFETs [15].



(a) (b)

Fig. 2. I_{ds}-V_{ds} of device simulations are compared against model prediction for an *n*-channel FinFET with device parameters in Table I and 45nm channel length for a) *on*-current b) Subthreshold current when V_{gs}=0.

The FinFET *on*-currents as a function of V_{ds} are given in Fig. 2(a) which reveals a good accuracy for the model.

C. Subthreshold Current

The major components of the static leakage current for FinFET transistors include both the gate tunneling and subthreshold currents. The front-gate leakage is nearly independent of the back-gate in asymmetrical DG transistors. It was shown by device simulation that by variation of the back-gate voltage between 0 and V_{dd}, the front-gate leakage had a variation of less than 5% but the subthreshold leakage varied between two and three orders of magnitude because of the strong dependence on the threshold voltage. Also, note that the use of high dielectric materials has lowered the gate tunneling current. In this work, we only consider the subthreshold current in the optimization of the standby power.

The subthreshold current in a double-gate FinFET can be expressed as [16]

$$I_{Dsub} = A\frac{H}{L_g}t_{si}\exp(\frac{V_{gs} - V_{thf}}{b})(1 - \exp(\frac{-qV_{ds}}{KT})). \quad (8)$$

where K is the Boltzmann constant, T is the temperature in Kelvin and, A and b are the fitting parameters. Fig. 2(b) shows a close match of the predicted subthreshold current in FinFET with the simulation results.

D. Read Stability

$V_{trip} - V_{read}$ can be considered as a good metric for the read stability of the cell [17]. For a stable read operation, it must be positive. V_{trip} can be found from the KCL equation at node L when VL and VR are set to V_{trip} as [17]

$$\begin{aligned} &I_{Dsat-NL}(V_{fg} = V_{trip}, V_s = 0, V_d = V_{trip}) \\ &= I_{Dsat-PL}(V_{fg} = V_{trip}, V_s = V_{dd}, V_d = V_{trip}) \\ &+ I_{Dsat-AL}(V_{fg} = V_{dd}, V_s = V_{trip}, V_d = V_{dd}). \end{aligned} \quad (9)$$

V_{read} may also be found from the KCL equation at node R during the read operation assuming VL to be V_{dd} as [17]

$$\begin{aligned} &I_{Dsat-AR}(V_{fg} = V_{dd}, V_s = V_{read}, V_d = V_{dd}) \\ &= I_{Dlin-NR}(V_{fg} = V_{dd}, V_s = 0, V_d = V_{read}). \end{aligned} \quad (10)$$

The read stability will be the highest if the back-gate voltages are set to zero. The reason is explained as follows. There are two ways to increase the read stability. First, we can increase V_{trip} which is achieved by increasing the threshold voltage of the pull up transistor and decreasing the threshold voltage of pull down transistor. Second, one should increase

the resistance of the access transistor and hence lower V_{read} which may be obtained by increasing the threshold voltage of the access transistors.

E. Write Stability

The write stability metric or write margin (*WM*) can be defined (for the case of Fig. 1) as the maximum *BLC* voltage that is able to flip the cell state while *BL* is kept high [6]. *WM* must be positive to consider the cell "*write stable*". In the write state, *PL* and *AL* divide the bitline voltage between each other. Assuming that there is not enough time for *VR* to increase and switch *NL* to the *on* state, *WM* can be calculated from the KCL at *VL* when *VL* is set to V_{trip} and *BLC* is set to the *WM* as

$$I_{ds-AL}(V_{fg}=V_{dd}, V_s=WM, V_d=V_{trip}) = I_{ds-PL}(V_{fg}=0\ , V_s=V_{dd}, V_d=V_{trip}). \quad (11)$$

We should find the region of operation of *AL* and *PL* at these biases to solve this equation. First, V_{trip} can be found as before from (9). $V_{Dsat\text{-}AL}$ and $V_{Dsat\text{-}PL}$ which are the drain saturation voltages can be found from (7). Comparing V_{trip} to $V_{Dsat\text{-}AL}$ and $V_{Dsat\text{-}PL}$, different regions of operation may be recognized. For example, if $V_{Dsat\text{-}AL} < V_{trip} < V_{Dsat\text{-}PL}$, we use the saturation current models for both transistors.

To increase the write stability, the access transistor should be strengthened while the pull down and pull up transistors should be weakened. This makes the back to back inverters weak and hence breaking the feedback becomes easier. So the optimum back-gate voltages are 1V, 0V, and 1V for the access, pull down, and pull up transistors, respectively.

G. Read Current

Read current is the indicator of the access time. As the read current increases, the access time decreases. In the read mode, the voltage of the node storing zero is raised to V_{read}. The current of the access transistor in this situation is the read current that discharges the proper bitline. This voltage lowering enables the sense amplifier to detects the zero and complete the read operation. The read current is considered as the saturation current of the access transistor when $V_{fg} = V_{dd}$, $V_s = V_{read}$, and $V_d = V_{dd}$. V_{read} can be calculated using (10).

The value of the bitline capacitance is estimated from our previous work and simulation results as 22.5fF [10]. The minimum read current can be obtained easily from (12). Δmin is set to be 0.1V in this paper.

$$I_{min} = \frac{C_{bitline}\Delta min}{T_{max}}. \quad (12)$$

In our model, while the pull up transistor does not have any effect on the access current, the pull down transistor should be chosen as strong as possible for reducing V_{read} and enhancing the overdrive voltage of the access transistor. Increasing the strength of the access transistors will yield two contradictory results; it increases its drive capability while at the same time it increases V_{read} and decreases the overdrive voltage of access transistor. The simulation results revealed that the former effect is the dominant one, and hence, the choice of the back-gate voltages as 1V for both the access, and pull down transistors will lead to the highest read current.

H. Subthreshold Leakage Power

Consider the SRAM cell shown in Fig. 1. When $VL = V_{dd}$ and $VR = 0$, the right access, left pull down, and right pull up transistors have subthreshold leakage. If the values of the storage nodes are complemented, the other three transistors will consume subthreshold leakage power.

In SRAM arrays, we can assume symmetric cases where half of the cells have stored "1" and the other half have stored "0" [17]. The subthreshold leakage power can be modeled as

$$StaticPower = \frac{1}{2}(I_{Dsub-AR}(V_{fg}=0, V_s=0, V_d=V_{dd}) + I_{Dsub-NR}(V_{fg}=0, V_s=0, V_d=V_{dd}) + I_{Dsub-PR}(V_{fg}=V_{dd}, V_s=V_{dd}, V_d=0) + I_{Dsub-AL}(V_{fg}=0, V_s=0, V_d=V_{dd}) + I_{Dsub-NL}(V_{fg}=0, V_s=0, V_d=V_{dd}) + I_{Dsub-PL}(V_{fg}=V_{dd}, V_s=V_{dd}, V_d=0)). \quad (13)$$

Since V_{dd} is equal to 1V, the subthreshold current may be considered as the subthreshold power (static power). High power consumption may not lead to functional failures but it will shorten the battery lifetime. In this work, we assume that our subthreshold power budget is 2μA per cell [18].

IV. Optimization Methodology

In this section, first, we discuss the random parameters in the SRAM cell. In addition, we describe a simple yield function used in our optimization. Finally, the implementation details of our optimization method are explained.

A. SRAM Probabilistic Variables

The channel length (L_g) and the silicon thickness (T_{Si}) of FinFETs are considered to be the major sources of the parametric variations in FinFETs [6]. The variations can be divided into local and global variations. The local variations are uncorrelated ($r = 0$) while the global variations of neighboring transistors are assumed to be completely correlated ($r = 1$) [19]. The local and global variances of L_g and T_{Si} are estimated to be $3\sigma = 10\%$ of their nominal values. This estimation is derived from the data reported in [20]. These variations are approximated to be Gaussian [20]. It should be noted that since the channel in the devices is lightly doped, random dopant fluctuation can be ignored. To consider the imperfection in the circuit that produces the back-gate voltages, we considered a standard deviation of 0.05V for each of these voltages. Thus, we have 30 random variables in the optimization space. Among them, 12 variables represent local variations and 12 variables represent global variations of L_g and T_{Si}. The remaining six variables represent different back-gate voltages. Note that nominal values of L_g and T_{Si} are determined by the technology while the optimization process provides us with the optimum values of the back-gate voltages.

B. Yield Modeling

In Section III, models for each SRAM metrics were proposed. We assume that each metric has a Gaussian distribution which is related to the 30 random variables via a function. Denoting the metric by y, we may write

$$y = f(x_1, \ldots, x_{30}). \quad (14)$$

where $x_1,\ldots,x_{30}$ are the Gaussian random variables with averages of $\eta_1,\ldots,\eta_{30}$ and standard deviations of $\sigma_1,\ldots,\sigma_{30}$. $r_{(i,k)}$ is the correlation coefficient between x_i and x_j. The mean and variance of the random variable y can be estimated as [17]

$$\mu_y = f(\eta_1,\ldots,\eta_{30}) + \frac{1}{2}\sum_{i=1}^{30}\frac{\partial^2 f}{\partial x_i^2}\Big|_{\eta_i}\sigma_i^2 + \sum_{k=1}^{30}\sum_{i=1;i\neq k}^{30}\frac{\partial^2 f}{\partial x_i \partial x_k}\Big|_{\eta_i,\eta_k} r_{(i,k)}\sigma_i\sigma_k. \quad (15)$$

$$\sigma_y^2 = \sum_{i=1}^{30}\left(\frac{\partial f}{\partial x_i}\Big|_{\eta_i}\right)^2\sigma_i^2 + 2\sum_{k=1}^{30}\sum_{i=1;i\neq k}^{30}\left(\frac{\partial f}{\partial x_i}\Big|_{\eta_i}\right)\left(\frac{\partial f}{\partial x_k}\Big|_{\eta_k}\right)r_{(i,k)}\sigma_i\sigma_k. \quad (16)$$

We define each metric such that if it is positive, there will be no failure. The read and write stability metrics already have this condition (by assuming zero noise margin as in [17]), and hence, we only need to redefine the read current metric as

ReadCurrent (New) = ReadCurrent (Old) – I_{min} (17)

where I_{min} is obtained from (12). Therefore, the failure probability for each metric is defined as

$$P[y_F] = P[y < 0]. \quad (18)$$

The general failure probability is defined as

$$P[All] = P[R_F + W_F + A_F] = P_{RF} + P_{WF} + P_{AF} - P[A_F R_F] - P[A_F W_F]. \quad (19)$$

where R_F, W_F, and A_F are the read, write, and access time failures, respectively. To evaluate (19), we need to have the joint CDF of y and z which is given by

$$P[y \le 0, z \le 0] = \int_{y=-\infty}^{0}\int_{z=-\infty}^{0} N_{y,z}(y:\mu_y,\sigma_y;z:\mu_z,\sigma_z)\,dydz$$

$$N_{y,z}(y,z) = \frac{1}{2\pi\sigma_y\sigma_z\sqrt{1-\rho^2}} \times \exp\left[-\frac{\left(\frac{y-\mu_y}{\sigma_y}\right)^2 - 2\rho\left(\frac{y-\mu_y}{\sigma_y}\right)\left(\frac{z-\mu_z}{\sigma_z}\right) + \left(\frac{z-\mu_z}{\sigma_z}\right)^2}{2(1-\rho^2)}\right]. \quad (20)$$

The correlation coefficient ρ can be computed from

$$\rho = \frac{E(yz) - E(y)E(z)}{\sigma(y)\sigma(z)} = \frac{E(yz) - \mu_y\mu_z}{\sigma(y)\sigma(z)}. \quad (21)$$

where yz is a function of 30 variables and $E(yz)$ can be found from (15).

In our calculations, we assumed that $P[R_F W_F]$ was negligible and the probability of simultaneous occurrence of three failures was zero. Finally, the yield may be found from

$$Yield = 1 - P[ALL]. \quad (22)$$

C. Yield Optimization

Based on the above discussion, our problem is converted to finding the maximum of the yield in the design. To find the optimum point in the parametric space, any nonlinear or evolutionary optimization technique can be employed. Evolutionary algorithms have the advantage of faster convergence and lower probability of being trapped in local optima. Particle Swarm Optimization (PSO) has been used in this paper as the engine of optimization due to ease of implementation and having continuous variables [21]. The algorithm is initiated by placing handful of agents with random velocity and location in the space of parameters. Their locations and velocities are modified using the following equation [21] after each iteration:

$$V_{id} = W_{inertia}V_{id} + C_1 rand()(P_{id} - X_{id}) + C_2 rand()(P_{gd} - X_{id}) \quad (23)$$

$$X_{id} = X_{id} + V_{id}.$$

where, C_1 and C_2 are constants, the *rand*() is a function which returns a value from a uniform distribution between 0 and 1, X_{id} and V_{id} are the location and velocity of each agent, $W_{inertia}$ is the inertia weight of the algorithm, P_{id} is the location of the best place that any agent has encountered in the whole time of the simulation, and P_{gd} is the location of the best global point in the parameter space that all the agents have found in the current iteration. As can be seen from the above formula, each agent has a memory which saves the best location that it has found so far and pursues it in its subsequent moves. Also, all the agents are capable of broadcasting their best found location to their neighborhood. The value of the yield function of (22) is taken as the fitness function of the evolutionary algorithm. The agents were defined as points in a three dimensional space where each dimension represents the back-gate voltage of one of access, pull down, or pull up devices. The search space is also confined by the maximum allowable leakage power which was chosen to be 2μW in this work.

V. Results and Discussion

The optimization process was applied to 45nm and 55nm channel lengths where we assumed the same process parameters (as given in Table 1). T_{max} was selected to be 75ps [17] for the channel length of 45nm and 100ps for the channel length of 55nm to compensate for the decreased strength due to the channel length increase. The optimum back-gate voltages obtained from the PSO algorithm are provided in Table II. Fig. 3 compares the yield for the optimized cell with that of tied-gates one. The results, which were obtained after 10,000 Monte Carlo simulations, show that the proposed technique increases the yield by 8.8% and 0.8% for the channel lengths of 45nm and 55nm, respectively. For the optimized cases, the yields are about 98% and 99%, respectively.

Fig. 4 shows how much failure probabilities change after the application of our technique. For the optimized cell, the main failure mechanisms (read and write failures) have decreased considerably while the access time failure has increased. Here, the read and write failures have decreased by increasing V_{trip} and the strength of the access transistors, respectively. The write failure is the main failure component in the tied-gates cell as shown in Fig. 4. This is due to surface orientation effects, which result in more symmetric nFET and pFET, and hence, a harder write operation for the tied-gates cell [15]. The access time failure in the tied-gates cell is lower because during the read operation, the back-gate of both pull down and access transistors are connected to the front-gate which is connected to V_{dd}. This results in the highest read current and lowest access time failure. However, in the

optimized cell, these voltages have lower values than V_{dd}.

Table II. Back gate voltages of the optimal cell.

Tr.	Back-Gate Voltage	
	L_g=45nm	L_g=55nm
Pull up	0.05V	0.0V
Pull down	0.05V	0.15V
Access	0.85V	0.9V

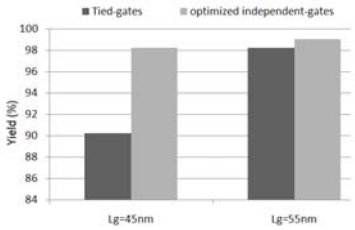


Fig. 3. Yield comparison of optimized and tied-gates SRAM cells for 45 and 55nm channel lengths.

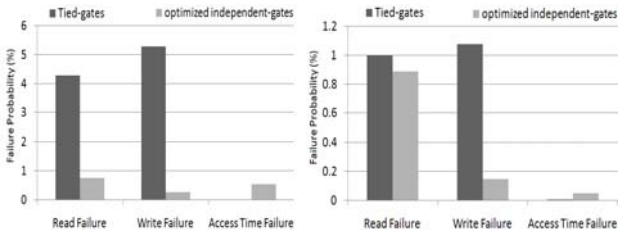


Fig. 4. Failure probabilities components of the tied-gates and optimized independent-gates SRAM cells, a) 45nm, b) 55nm.

To study the effect of the local and global variations on the failure components, each of these variations were applied independently to our optimized cell for the 45nm channel length. The results are shown in Fig. 5. The read and write failures happen due to the mismatch in the cell transistors [17]. As the results show, the read and write failures are mainly due to the local variations which induce mismatch. On the other hand, the global variations give rise to more access time failures. The reason is that if the strength of the access or pull down transistor decreases, the strength of the other transistor also decreases enlarging the access time failure. Note that the sum of the two access time failures is less than that when they are applied simultaneously. This shows that access time failure depends more on the strength variation of the access or pull down transistor than on the relative strength variation of these transistors [17].

VI. Conclusion

A method for optimizing the design of double-gate FinFET based SRAMs was presented. The method used a statistical optimization process to maximize the yield against process variations. SRAM read, write, and access time failure metrics were modeled and then the optimum back-gate voltages were found using particle swarm optimization. It was shown that by modulating the back-gate voltage of the three kinds of transistors in the SRAM cell, a much higher yield than the tied-gates version is achievable. The increase in the yield was 0.8% and 8.8% for the cells with the channel lengths of 55nm and 45nm, respectively. This shows the effectiveness of the proposed techniques increases as the devices shrinks.

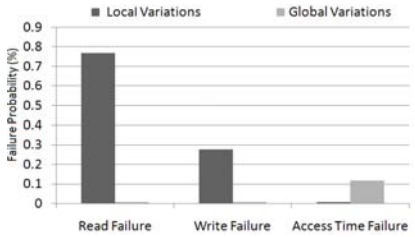


Fig. 5. The probabilities of failure components of the optimized independent-gates SRAM cells for the 45nm channel length due to local and global variations.

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