7nm FinFET Standard Cell Layout Characterization and Power Density Prediction in Near- and Super-Threshold Voltage Regimes

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Abstract—In this paper, we present a power density analysis for 7nm FinFET technology node, including both near-threshold and super-threshold operations. We first build a Liberty-formatted standard cell library by selecting the appropriate number of fins for the pull-up and pull-down networks of each logic cell. The layout of each cell then is characterized based on the lambda-based layout design rules for FinFET devices. Finally, the power density of the 7nm FinFET technology node is analyzed and compared with the state-of-the-art 45nm CMOS technology node for different circuits. Hspice results show that the power density of each 7nm FinFET circuit is at least 10 to 20 times larger than that of the same 45nm CMOS circuit in near- and super-threshold voltage regimes. Also the power densities of FinFET circuits are shown to be much higher than the limit of air cooling, which necessitates careful thermal management for the FinFET technology.

I. INTRODUCTION

The growing packing density and power consumption of VLSI circuits have made thermal effect an increasingly important concern of VLSI designers [1]. The need to reduce power consumption in VLSI circuits and meet thermal constraints is driving the push toward ultra-voltage scaled CMOS designs, i.e., circuits that operate at near/sub-threshold supply voltage levels [2][3]. In addition, with the dramatic downscaling of layout geometries, the traditional bulk CMOS technology is facing significant challenges due to several reasons such as the increasing leakage and short-channel effects (SCEs) [4]. FinFET devices, a special kind of quasi-planar double gate devices, have been proposed as an alternative for the bulk CMOS when technology scales beyond the 32nm technology node [5][6]. It has been reported that FinFET devices offer superior scalability [7], lower gate leakage current [8], excellent control of short-channel effects [9], and relatively immunization to gate line-edge roughness [10].

Due to the promising future of the nanoscale FinFET devices, considerable research efforts have been made in their modeling and characterizing. Sinha et. al. presented a Predictive Technology Model for multi-gate transistors (PTM-MG) for FinFETs in sub-20nm technology nodes [11] which is based on BSIM-MG model presented in [12]. An alternative approach based on fundamental physics principle is adopted by Gupta et. al, and generates FinFET device models at 5nm [14]. A lookup-table(LUT)-based model is presented in [14], which is compatible with SPICE through the Verilog-A interface.

Although the behavior of FinFET devices has been well researched, none of the previous works have focused on the thermal-effect analysis of future ultra-scaled FinFETs. To address the strong and direct impact of power-density on the thermal characteristics of VLSI circuits, we present a power density analysis for FinFET 7nm technology node, including both near-threshold and super-threshold operations. We first build a Liberty-formatted standard cell library [15] by selecting the appropriate number of fins for the pull-up and pull-down networks of the logic cells. After that, We use the lambda-based layout design rules to characterize the FinFET logic cell layout. All cell layouts are designed using the same height to help with floorplanning flexibility and eventually area reduction. Finally, the power density of the 7nm FinFET technology node is analyzed and compared with the state-of-the-art 45nm CMOS technology node for different ISCAS benchmarks by calculating the ratio of total power consumption and estimated area. Hspice results confirm that the power density of a circuit in 7nm FinFET node can be at least 10 to 20 times larger than that in 45nm CMOS node in both near- and super-threshold voltage regimes. The results also indicate that the power densities of FinFET circuits can easily surpass the limit of air cooling designs. This in turn demands a careful thermal management for FinFET technologies. To the best of our knowledge, this is the first paper that deals with power density of FinFET devices.

The rest of this paper is organized as follows. Section II introduces the properties of 7nm FinFET devices at multiple supply voltages. Section III explains the library format and characterization flow. The layout characterization details are elaborated in Section IV. We show the synthesis results as well as the power density reports in Section V and conclude the paper in Section VI.

II. 7NM FINFET TECHNOLOGY NODE

FinFET devices show better suppression of the short channel effect, lower energy consumption, higher supply voltage scaling capability, and higher ON/OFF current ratio compared with the bulk CMOS counterparts [16]. Figure 1 shows the structure of a 7nm FinFET device. The FinFET device consists of a thin silicon body, with thickness of T_{fin},

which is wrapped by gate electrodes. The device is termed quasi-planar as the current flows in parallel with the wafer plane, and the channel is formed perpendicular to the plane. The effective gate length L_G is twice as large as the fin height h_{fin}. The spacer length L_{SP} is an important design parameter that directly relates to the short channel effects [14]. The FinFET structure allows for fabrication of separate front and back gates. In this structure, each fin is essentially the parallel connection of the *front-gate-controlled FET* and the *back-gate-controlled FET*, both with a width equal to the fin height h_{fin}. A unique feature of FinFET devices is the *independent gate control*, where the front and back gates can be tied to the same or different control signals. In this paper, we use the shorted gate mode in FinFET device model developed in [14], in which the front gate and back gate are tied together. FinFETs operating in this mode offer the highest driving strength [17].
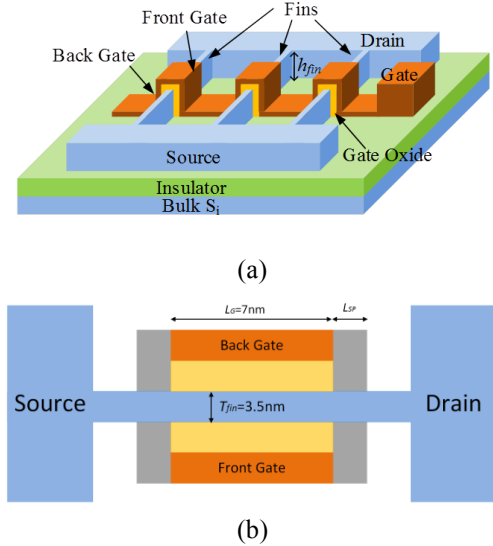

(a)

(b)

Figure 1. (a) Perspective view and (b) top view [14] of the 7nm FinFET device.

In this paper, we study the characteristics of 7-nm FinFET devices operating in both super- and near-threshold supply voltage regimes. Near-threshold operation regime achieves reduced energy consumption at the cost of degradation of circuit speed. When the supply voltage V_{dd} is reduced, the dynamic energy consumption reduces quadratically. However, the leakage energy consumption, which is the product of leakage power and circuit delay, increases because the increase of the circuit delay (satisfying an exponential relation versus V_{dd}) surpasses the reduction of leakage power (satisfying a linear relation versus V_{dd}). To enable both low power and high performance applications, we perform power density analysis under two supply voltages: 0.3V for near-threshold regime and 0.45V for super-threshold regime.

III. STANDARD CELL LIBRARY CHARACTERIZATION

To perform thermal analysis on a given circuit, the gate-level implementation of the circuit is needed, which requires characterization of standard cell library. A standard cell library is a set of high-quality timing and power models that accurately and efficiently capture the behavior of standard cells. The standard cell library is widely used in many design tools for different purposes, such as logic synthesis, static timing analysis, power analysis, high-level design language simulation, and so on, as part of Computer-Aided-Design (CAD). The Liberty library format (*.lib*), which was first invented by Synopsys a decade ago, has become an industrial standard that is adopted by over 100 semi-conductor vendors and implemented in over 75 production electronic design automation (EDA) tools [18]. Therefore, we build our 7nm FinFET standard cell library in the .lib format.

The main goal of this paper is to analyze the power density and the resulting thermal effect. Therefore, the area power consumption estimation of a certain FinFET circuit is of great interest. In this section, we discuss the standard cell sizing and power parameter characterization in detail. Other parameters such as propagation delay, transmission time, setup time and hold time of flip-flops are also necessary for standard cell library characterization but are omitted because of space limit.

A. Standard Cell Sizing

The drive strength of a FinFET device depends on the ratio of fin height and channel length, while both parameters are determined by the fabrication technology. Thus, the FinFET standard cell sizing involves selecting the appropriate number of fins for the pull-up network and pull-down network of each logic cell.

The general sizing method is to balance the rise and fall delays of a standard cell. We first investigate the numbers of P-type fins and N-type fins in an inverter that achieve approximately equal rise and fall delays. According to the transregional FinFET model [19], the drain current of a FinFET in the sub- and near-threshold regimes is given by

$$I_{ds} = I_0 e^{\frac{(v_{gs}+\lambda V_{ds}-V_{th})-a(V_{gs}+\lambda V_{ds}-V_{th})^2}{m\cdot v_T}}(1-e^{\frac{-V_{ds}}{v_T}}) \quad (1)$$

where λ is the drain voltage dependeny coefficient (similar to but much smaller than the DIBL coefficient for bulk CMOS devices), v_T is the thermal voltage, and I_0, a, and m are technology-dependent parameters to be derived using Hspice simulation.

In order to achieve equal rise and fall delay, the number of P-type fins N_P in an inverter can be determined by

$$N_P = N_N \cdot \frac{I_{ds,N}}{I_{ds,P}} \quad (2)$$

where $I_{ds,N}(I_{ds,P})$ is the drain current of an N-type(P-type) fin when $|V_{gs}| = |V_{ds}| = V_{DD}$, and N_N is the number of N-type fins in the inverter.

In order design other combinational logic cells under near-threshold regime, we need to solve the *stack sizing* problem. In some logic cells, there are several transistors connected in series forming a *stack*, e.g., the pull-down network of a NAND or the pull-up network of a NOR. The stack sizing problem involves determining the transistor sizes in a stack such that the logic cell achieves equal rise and fall delays. We use the 2-input NAND1X as an example. Figure shows an INV1X and a 2-input NAND1X, and the number on top of a

FinFET transistor symbol denotes the number of parallel-connected fins in that FinFET transistor. The INV1X achieves equal rise and fall delays in the near-threshold regime. We denote the stack sizing factor in an m-input NAND by $\rho_{N,m}$, where the subscript N denotes N-type FinFET devices. Similarly, the stack sizing factor in an m-input NOR is denoted by $\rho_{P,m}$. The stack sizing factor $\rho_{N,2}$ of the 2-input NAND is defined as the ratio of the number of N-type fins connected to an input signal in the 2-input NAND1X to that in the INV1X, such that the pull down network of the 2-input NAND1X has the same current driving strength as that in the INV1X. From the theoretical calculation based on FinFET model (1) and Hspice simulation, we obtain $\rho_{N,2} = 3.25 \approx 3$ in the near-threshold regime. Please note that $\rho_{N,2}$ is larger than 2, which is the typical value for bulk CMOS in the super-threshold regime. Similarly, we can obtain $\rho_{P,2} = 3$, $\rho_{N,3} = 6$, and $\rho_{P,3} = 5$. Please note that a stack of more than 3 transistors may not be favored in the near-threshold circuits because of significant performance degradation.
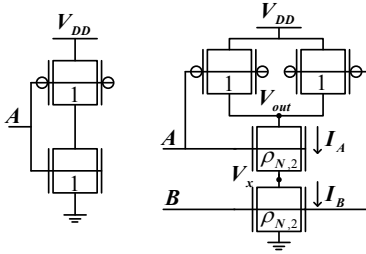

Figure 2. Illustration of stack sizing for a 2-input NAND.

With the sizing of INV's and derived stack sizing factors, the sizing of all the rest combinational logic cells and the sequential logic cells can be derived accordingly. All the logic cells included in the 7nm FinFET standard cell library are summarized in Table I. The functionality of each logic cell is verified by HSPICE simulation. Please note that we use the same sizing of FinFET logic cells in the super-threshold regime ($V_{DD} = 0.45$ V), since we assume our standard cells support DVFS (dynamic voltage and frequency scaling).

TABLE I. SUMMARY OF LOGIC CELLS INCLUDED IN 7nm STANDARD CELL LIBRARY

	Cell type	Scale/triggering
Combinational logic cells	Inverter	1X, 2X, 4X, 8X
	2-input NAND	1X, 2X, 4X, 8X
	3-input NAND	1X, 2X, 4X
	2-input NOR	1X, 2X, 4X, 8X
	3-input NOR	1X, 2X, 4X
	AND-OR-INV	1X, 2X, 4X
	OR-AND-INV	1X, 2X, 4X
	XNOR	1X, 2X,
	XOR	1X, 2X,
	MUX	1X, 2X
Sequential logic cells	Latch	Active-high
	D-flip-flop	Positive-edge
	D-flip-flop w/ S/R	Positive-edge

B. Power Parameter Characterization

The power parameters in the Liberty library include the leakage power and internal power of a logic cell. The overall power consumption is evaluated by summing up the leakage power, *internal power*, and switching power (power consumed when charging and discharging the capacitive load). The internal power accounts for the short-circuit power consumption and dynamic power of the diffusion capacitors at the output pin of the logic cell. 2D LUTs are used to store internal power values of the output pin related to each input pin.

We measure the leakage power consumption by multiplying the supply voltage to the average current flowing out from the V_{dd} terminal when there is no input and output signal transition,

$$P_{leak} = V_{dd} \times average\big(I(V_{dd})\big) \qquad (3)$$

For combinational logic cells, the internal power is measured by subtracting the switching energy at the capacitive load from the total energy consumption when output signal transits, which is calculated by integrating the outgoing current of V_{dd} from the beginning of the input transition ($t_{in,start}$) to the end of the output transition ($t_{out,end}$). Note that switching energy is only consumed when the capacitive load gets charged.

$$E_{fall} = V_{dd} \cdot \int_{t_{in,start}}^{t_{out,end}} I(V_{dd})dt$$

$$E_{rise} = V_{dd} \cdot \int_{t_{in,start}}^{t_{out,end}} I(V_{dd})dt - C_{load}V_{dd}^2$$

$$\qquad (4)$$

Measuring the internal power for sequential logic cells is complicated because clock signal and data signal both result in energy consumption when they switch to high and low. Therefore, we design a waveform such that we can measure the energy consumption for different combinations of clock, data, and output signals, as shown in Figure . Each energy term in Figure is measured by multiplying the supply voltage to the current integral over that short time interval.
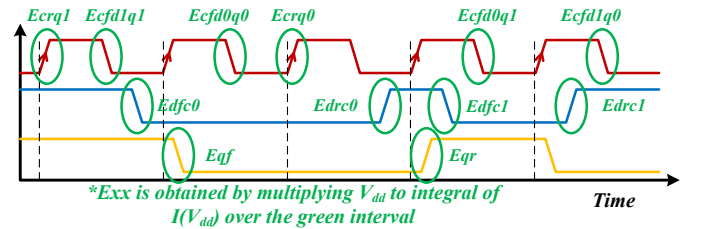

Figure 3. Characterizing the internal power of a D-flip-flop.

We first measure the internal power of the rising clock edge, denoted by E_{crise}, without causing the output voltage change. Two energy values are measured when output stays at 0 (E_{crq0}) and 1 (E_{crq1}), respectively. Thus, we have,

$$E_{crise} = (E_{crq0} + E_{crq1})/2 \qquad (5)$$

The falling edge of clock does not trigger the change of the output signal, therefore, we consider all four combinations of signal at the data pin and output pin. The internal power of the

falling clock edge (E_{cfall}) is an average value of energy measured when clock falls and the (data, output) is (0, 0), (0, 1), (1, 0), and (1, 1), respectively.

$$E_{cfall} = \left(E_{cfd0q0} + E_{cfd0q1} + E_{cfd1q0} + E_{cfd1q1}\right)/4 \quad (6)$$

The data signal may switch when the clock is high or low. We calculate the rising (E_{drise}) and falling internal power (E_{dfall}) of data signal as follows,

$$E_{drise} = (E_{drc0} + E_{drc1})/2$$
$$E_{dfall} = (E_{dfc0} + E_{dfc1})/2 \quad (7)$$

The output pin voltage transits at the rising clock edge. Thus, to avoid double counting, we subtract the internal power of rising clock edge to obtain the internal power for rising (E_{qrise}) and falling output (E_{qfall}).

$$E_{qrise} = E_{qr} - E_{crise} - C_{load}V_{dd}^2$$
$$E_{qfall} = E_{qf} - E_{cfall} \quad (8)$$

IV. 7NM FINFET LAYOUT CHARACTERIZATION

After the standard library is characterized, we design the layout of each cell based on the lambda-based layout design rules for FinFET devices. In this section, we first present the layout of each standard cell based on the sizing result of the previous section. We use the layout of logic cells to analyze the interconnection of different cells to estimate the total area consumption of a given circuit.

A. FinFET Layout Design Rules

General understanding of the FinFET layout density is challenged by its dependence on the specific technology adopted to manufacture the "fin" (which is the core of FinFET) [20]. As discussed in the previous sections, we focus on the layout of FinFET devices operating in the shorted gate mode. Figure 4 shows the comparison between the layout of a general CMOS device and a shorted gate FinFET device with four fins. In this FinFET layout structure, a single strip is used for the gate terminal, while source and drain terminals of multiple fins are connected together through a metal wire to make a wider FinFET device. This is different from CMOS devices.
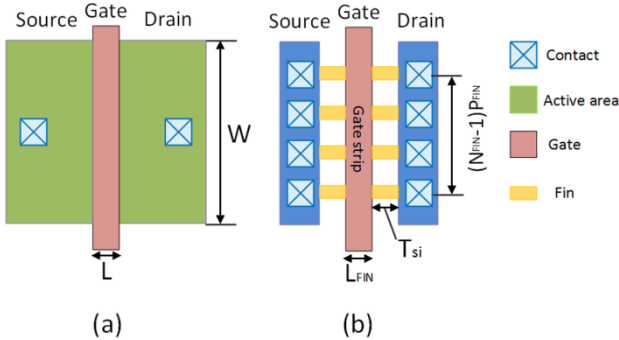

Figure 4. Layout of (a) a general CMOS device and (b) a shorted gate FinFET device with four fins.

In this section, we used the modified lambda-based layout design rules to characterize the layout of each FinFET logic cell. Authors in [22] have reported the major process-related FinFET geometries for 5nm technology and similar values can be derived for 7nm technology, which is shown in Table II. The detailed process design rules are also included in this table. Notice that generally the layout design rules are similar for CMOS and FinFET technologies because the major difference is on fin fabrication [21]. One critical process-related geometry for FinFET devices shown in Figure 4 is the *fin pitch*, P_{FIN}, which is defined as the minimum center-to-center distance of two adjacent parallel fins. The value of P_{FIN} is determined by the underlying FinFET technology. More precisely, there are two types of FinFET technologies: (1) *Lithography-defined* technology where lithographic constraints limit the fin pitch spacing, and (2) *spacer-defined* technology which relaxes the constraints on P_{FIN}, and obtains 2x reduction in the value of P_{FIN} at the cost of a more elaborate and costly lithographic process [23]. In this paper, we focus on the layout characterization of 7nm Lithography-defined technology and perform the corresponding estimation for the spacer-defined technology.

TABLE II. FINFET-SPECIFIC GEOMETRIES AND DESIGN RULES

Parameter	Value in 7nm FinFET (nm)	Value in 5nm FinFET (nm)	Comment
L_{FIN}	$2\lambda=7$	$2\lambda=5$	Fin length
T_{SI}	3.5	2.725	Fin width
H_{FIN}	14	10.9	Fin height
P_{FIN}	$2\lambda+T_{SI}=10.5$	$2\lambda+T_{SI}=7.5$	Fin pitch using spacer lithography
t_{ox}	1.55	1.09	Oxide thickness
W_C	$3\lambda=10.5$	$3\lambda=7.5$	Minimum contact size
W_{M2M}	$3\lambda=10.5$	$3\lambda=7.5$	Minimum space between metal wires
W_{G2C}	$2\lambda=7$	$2\lambda=5$	Minimum space of gate to contact

B. 7nm FinFET Standard Cell Characterization

Based on FinFET-specific geometries and design rules, the layouts of standard cells can be determined according to the sizing results of each logic cell, which has been shown in Section III.A. To achieve higher layout flexibility, the number of fins for certain cells has been slightly adjusted. In addition, considering both area consumption and floorplanning flexibility, all the standard cell layouts are designed with the same height. We set the height of all the cells the same as the standard 2-input 2X NAND cell in order to achieve the best tradeoff between design flexibility and area waste. The shared

diffusion and width extension can be used when we design the layout of larger cells. Figure 5 shows the layout geometry of some basic cells with different sizes. In our standard cell library, all the gates are designed with a fixed height of 54λ. Inverter 1X, 2X and 4X gates achieve an active width of 27λ and the 2-input NAND gates of both 1X and 2X sizes have an active width of 27λ. The 8X inverter and 2-input 4X NAND gate have active widths of 27λ and 45λ respectively by using shared diffusion and width extension. 2-input NOR gate has the same area consumption as 2-input NAND gate of the corresponding size. Notice that the active width has already included the layout interconnect overhead, which is shared by 6λ per cell.
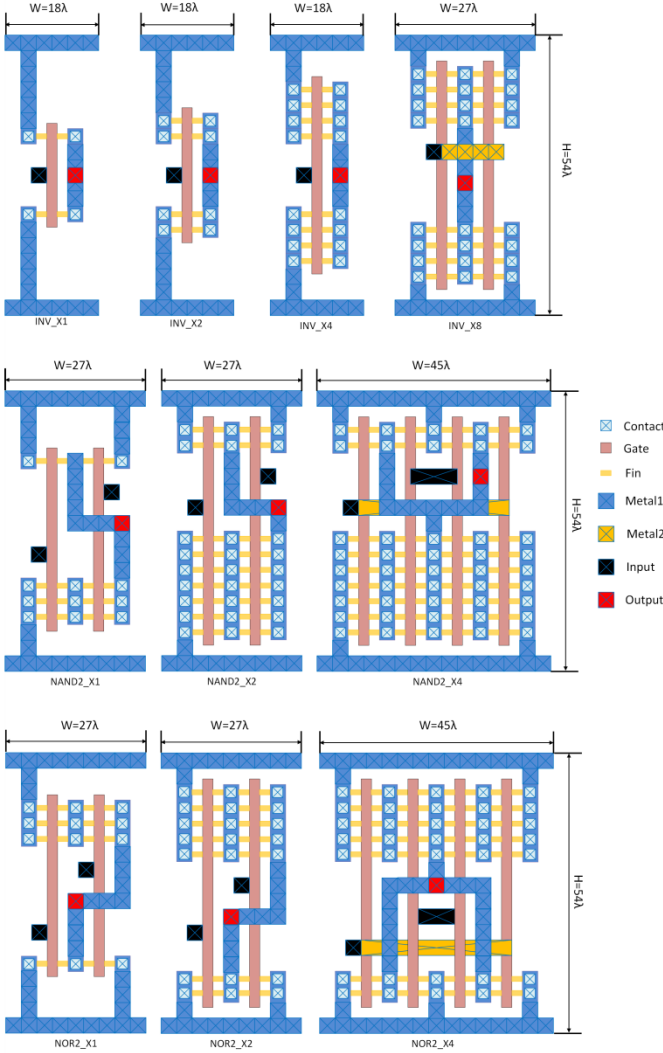

Figure 5. 7nm FinFET layout geometry of inverters, 2-input NAND gates and 2-input NOR gates with different sizes

Another standard cell layout design rule is to align the input and output ports to make it easier for interconnection, especially for the global signals (e.g. the clock signal of latches and flip-flops). Figure 6 shows the layout design of a latch, which sacrifices some area in order to align the clock signal. This clock signal might be connected to other sequential logic cells. The active width of the latch is 90λ,

which is a little more than the minimal achievable width (around 80λ based on our trials). But it makes it much easier for global routing.
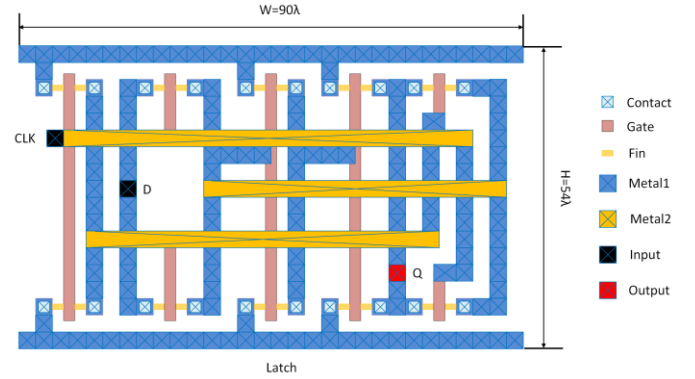

Figure 6. 7nm FinFET layout design of a latch

According to the FinFET-specific layout design rules as well as our fixed-height design method, the layout of combinational logic cells and the sequential logic cells can be derived accordingly. The geometries of all the logic cells included in the 7nm FinFET standard cell library are summarized in Table III.

TABLE III. 7nm FINFET STANDARD CELL LAYOUT GEOMETRIES

Cell type	Scale/triggering	Active width (λ)
Inverter	1X, 2X, 4X, 8X	18, 18, 18, 27
2-input NAND	1X, 2X, 4X, 8X	27, 27, 45, 81
3-input NAND	1X, 2X, 4X	36, 63, 117
2-input NOR	1X, 2X, 4X, 8X	27, 27, 45, 81
3-input NOR	1X, 2X, 4X	36, 63, 117
AND-OR-INV	1X, 2X, 4X	36, 63, 117
OR-AND-INV	1X, 2X, 4X	36, 63, 117
XNOR	1X, 2X,	60, 87
XOR	1X, 2X,	60, 87
MUX	1X, 2X	81, 129
Latch	Active-high	90
D-flip-flop	Positive-edge	156
D-flip-flop w/ S/R	Positive-edge	192

V. SYNTHESIZE RESULTS AND POWER DENSITY ANALYSIS

In order to predict the power density values in 7nm FinFET technology, we synthesize various ISCAS benchmark circuits using the developed FinFET standard cell library in both super threshold (Vdd=0.45V) and near threshold (Vdd=0.3V) regimes. The power density value is calculated as the ratio of power consumption and the total area of the circuit. We use 45nm CMOS technology for comparison because there are widely-received libraries and thermal analysis results in this technology node. The same circuits are synthesized using the 45nm CMOS library developed by North Carolina State University (NCSU) [24]. All benchmark circuits are synthesized by Synopsys Design Compiler [25].

TABLE IV. POWER DENSITY REPORT OF DIFFERENT ISCAS BENCHMARKS

Circuit	FinFET 7nm Vdd=0.3V			FinFET 7nm Vdd=0.45V			NCSU 45nm Vdd=1.1V		
	Average power (uW)	Total area (um^2)	Power density (mW/mm^2)	Average power (uW)	Total area (um^2)	Power density (mW/mm^2)	Average power (uW)	Total area (um^2)	Power density (mW/mm^2)
c432	9.32	6.76	1380	12.7	5.96	2131	78.9	625	126.3
c499	21.72	17.3	1256	30.8	12.4	2484	78.7	922.8	85.3
c880	11.6	15.3	757	18.9	8.93	2114	74.5	889	83.8
c1355	25.3	20.4	1241	31.3	12.2	2562	117.8	1167	100.9
c1908	26.0	15.3	1702	38.8	16.1	2410	106.9	993.1	107.7
c3540	53.5	35.6	1503	87.7	33.8	2591	396	2768	143

To estimate the power consumption of each circuit in reality, we assume the circuit is operating in a processor with a frequency of f and also we consider an activity factor α, which determines the circuit switching activity. The average power consumption of a circuit can be calculated using:

$$P_{average} = P_{leakage} + \alpha \cdot P_{dynamic} \cdot D \cdot f, \qquad (9)$$

where both the leakage power $P_{leakage}$ and the dynamic power $P_{dynamic}$ can be found in the power report from Design Compiler. The value D in this equation represents the circuit delay (which can be found in the timing report) and thus $P_{dynamic} \cdot D$ is the total energy consumption during one switch. In this paper, the α value is set to be 0.2 and we assume the circuit is operating under a frequency of 500Mz when estimating the average power consumption. Our estimated power density of 45nm CMOS technology matches the previously reported value, which is around 140mW/mm^2 [26].

Synopsys Design Compiler also reports the total cell area consumption during the synthesis process. In addition to that, we consider a cell area utilization value, which is the ratio of the total cell area and the total area including place and route as well as the spaces between cells. The cell area utilization value is set to be 80% according to [27].

Table IV summarizes the power, area and power density values for different ISCAS benchmarks. One can observe that the power density of 7nm FinFET circuits can reach over 1500mW/mm^2 in near-threshold regime and over 2500mW/mm^2 in super-threshold regime. These values are much higher than the limit of air cooling (around 1000mW/mm^2 [28]) and careful thermal management will be needed for FinFET devices. Notice that we are using an optimistic estimation for power density of FinFET devices in this paper because of the following two reasons: First, we assume the operating frequency is the same for 45nm CMOS and 7nm FinFET technologies, while in reality, FinFET circuits achieve a much better delay and thus the operating frequency can be higher than that of 45nm CMOS circuits [14]. Second, the layout geometry in this paper is based on *Lithography-defined* technology, and the use of *spacer-defined* technology, which relaxes the constraints on P_{FIN}, will further compress the layout size and thus increase the power density.

VI. CONCLUSION

FinFET devices outperform bulk CMOS devices in ultra-low power designs by allowing for higher voltage scalability. In this paper, we present a power density analysis for 7nm FinFET devices under multiple supply voltage regimes, considering both high performance and low power usage. A Liberty-formatted standard cell library is built and the layout of each cell is characterized based on the lambda-based layout design rules for FinFET devices. Finally, the power density of 7nm FinFET technology node is analyzed and compared with an advanced 45nm CMOS technology node for different circuits. Hspice results confirm that the power density of each 7nm FinFET circuit is at least 10 to 20 times larger than that of the same circuit in 45nm CMOS node. We have also shown that the power density of FinFET circuits can easily surpass the limit of air cooling. Therefore, careful thermal management will be needed for the 7nm FinFET technology.

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