Design and Optimization of a Reconfigurable Power Delivery Network for Large-Area, DVS-Enabled OLED Displays

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***Abstract*— Dynamic voltage scaling (DVS) has proven effective in minimizing the power consumption of OLED displays, resulting only in minimal image distortion. This technique has been extended to perform zone-specific DVS by dividing the panel area into zones and applying independent DVS to each zone based on the displayed content. The application of the latter technique to large-area OLED displays has not been done in part due to a high overhead of its dedicated DC-DC converter for each zone and low conversion efficiency when the load current of each converter lies outside the desirable range. To address this issue, this work proposes a reconfigurable power delivery network architecture, comprised of a small number of DC-DC converters, a switch network and an online controller, to realize fine-grained (zone-specific) DVS in large-area OLED display panels. The proposed framework consistently achieves high power conversion efficiency and significant energy saving while preserving the image quality. Experimental results demonstrate that up to 36% power savings can be achieved in a 65" 4K Ultra high-definition OLED display by using the proposed framework.**

Keywords Low-power design; OLED; Power delivery network;

I. Introduction

OLED (Organic Light Emitting Diode) has emerged as a promising light source for displays, and continuous progress in OLED displays has enabled their steady market growth. Among all OLED applications, the market of large-area OLED panels has been growing rapidly. The OLED TV is expected to be the second largest OLED application in 2017, with around $3 billion revenue following the mobile phone display with around $4 billions in annual revenue. In reality, enlarging the size of flat OLED panels has faced many technical setbacks in terms of panel fabrication and control. For example, occurrence of short circuits, non-uniformity of light emission, local heat generation and hot spots are the well-known problems in the large-area OLED panels [1]. However, extensive efforts by industry and academia have successfully overcome many of these fabrication issues by exploiting new materials and patterning techniques [2]. As a result, 65" 4K (UHD or Ultra High Definition) OLED panels have already been commercialized and are available in the market.

Low power efficiency of OLED displays remains a problem not only for large-area OLED panels but also for small portable panels. This is because of the power consumption characteristics of OLED cells: OLED is a surface-emitting lighting source, with each pixel comprised of red, green, and blue cells. Cells with different displayed colors have different power efficiencies and different power consumptions at a given luminance level. As a result, to display the black color, an OLED pixel (with red, green, and blue cells) consumes less than 40% the amount of power compared with an LCD pixel displaying black, whereas displaying white consumes almost three times as much power as that of a LCD pixel [3].

To tackle this issue, many power management methods have been proposed, which mainly focus on controlling the pixel color composition. Some examples are the *local dimming method* presented in [4], and the *color remapping method* in [5][6]. Furthermore, a supply voltage scaling method of OLED displays (OLED-DVS) has been proposed in [7] to reduce power waste in OLED pixel drivers. Given that the luminance of the OLED pixel is proportional to its driving current, this OLED-DVS method can maintain the image quality as long as the driving current of OLED pixels can be maintained regardless of the voltage scaling. The supply voltage control architecture and on-line control scheme for an image sequence has been introduced in [8], while the OLED-DVS technique has been applied to online movie streaming in [9]. Recently, the more aggressive approach for the OLED-DVS has been investigated in [3][10], which partitions a panel into several zones (sub-panels), and applies possibly different voltage levels to the different zones. Applying the OLED-DVS to each zone can take full advantage of power-saving that the DVS method can offer. Note that if DVS is applied to the whole panel, some regions of the panel may not need a high voltage level, but their voltage level can not be lowered due to the requirements of other regions. This method is called *zone specific* OLED-DVS.

Among the proposed methods, we pay attention to the zone-specific OLED-DVS, which is directly applicable to the large-area OLED display. In addition to improving the power efficiency, large-area OLED panels also benefit from fine-grained control of the zoned panel due to the reduced IR drop and the resulting enhanced image quality. The voltage distribution on power lines in large Active Matrix OLED (AMOLED) displays has been investigated as a function of panel size in [11]. It is reported that, due to the IR-drop, the supply voltage drops significantly as the panel size increases. Indeed, depending on the location of pixels and the paths of current flowing from the power supply to each individual pixel, the amount of the IR-drop may be different for different pixels. This phenomenon will ultimately affect the image quality due to non-uniformity of brightness. In recent large-area OLED panels, uneven distribution of supply voltage emerges as a critical problem [1]. To tackle this IR-drop problem, dividing a large panel into several sub-panels, each of which with a dedicated power line, has been introduced [12].

Unfortunately, to the best of our knowledge, there has been no study in the literature about how one can deliver multiple supply voltages to multiple sub-panels. To support an independent voltage control for each sub-panel, at least one DC-DC converter (called converter in the remainder of this paper) per sub-panel should be attached to the external power supply board or panel. Having a large number of converters gives rise to significant area, cost and power overheads by introducing a large number of inductors and capacitors [13][14]. For instance, as a panel is zoned with finer granularity, the required number of converters increases, and eventually exceeds the maximum allowable space. In addition, although state-of-the-art converters exhibit high peak efficiency, their efficiency can drop dramatically under adverse load conditions (i.e., out-of-range load current levels). Thereby, when many converters operate at low efficiency, the power loss of the converters becomes critical.

In this work, we present a power delivery architecture based on a reconfigurable switch network to maximize efficacy of the DVS method in large OLED panels with the minimum overhead. The proposed reconfigurable power delivery network (PDN) utilizes the minimum number of converters but achieves their full potential. The basic concept of the proposed PDN is that grouping some sub-panels to be powered by a single converter can reduce the converter power loss significantly. For example, if the sub-panels that require a relatively small amount of load current are grouped together, the single converter will have a relatively high load current. Due to the converter efficiency characteristic curve, the converter will exhibit higher efficiency. Of course, when grouping the sub-panels, we should also take into account the power consumption of sub-panels and power losses induced by IR-drop. Therefore, we also propose an optimization algorithm to control the proposed PDN to minimize power consumption

of the whole system. This algorithm is to optimally divide the sub-panels into the several groups, and perform group-level DVS.

We validate the proposed methods on an AMOLED panel model that we develop for the realistic experiment. We target a 65" TV platform that supports 4K UHD (4096 x 2160) resolution. We perform detailed simulations on the target platform with a commercial converter carefully selected for fair evaluation. Results demonstrate that up to 36% power savings can be achieved.

II. Dynamic voltage scaling (DVS) with the zoned, large-area OLED display panel

A. OLED-DVS

Like LCD panels, OLED display panels can be classified into two types: passive matrix OLED (PMOLED) and active matrix OLED (AMOLED). The PMOLED panels consist of simple driver structures, hence their manufacturing cost is low and the control scheme is relatively simple. However, the simple structure of the PMOLED panels inherently restricts the resolution to be low and panel size to be small (i.e., typically up to 3") [8]. In contrast, the AMOLED panels are driven by a thin-film transistor (TFT) with a storage capacitor, which enables large size and high resolution displays. In this work, we thus target the AMOLED panels for the large-area displays.

Lowering the supply voltage level V_{DD} to reduce power loss from the driver circuit in the panel is the key concept of the OLED-DVS. Typically, OLED drivers are designed to have 50% to 100% headroom between static V_{DD} and OLED cell voltage V_{cell}, so as to guarantee full contrast and luminance on the panel [7]. Nevertheless, V_{cell} seldom reaches its maximum value, and thus the large headroom results in low power efficiency of the OLED panel. In other words, OLED-DVS can be applied to most of displayed images, and the resulting power savings may be significant. References [3][8] presented a *DVS-friendly* AMOLED driver structure to enable the OLED-DVS in the panel, and achieved considerable power savings. We omit detailed explanation of the presented driver structure from [3][8] in this paper, but underline its key feature that enables V_{DD} to be scaled down to a certain degree while still satisfying the image quality.

Unfortunately, we cannot control V_{DD} values cell by cell or even pixel by pixel due to the implementation difficulties and expense (e.g., overhead of converters). Rather, DVS can be applied either to the overall panel [8] or to multiple sub-panels at finer granularity (the zone-specific OLED-DVS) [3][10][9]. This limitation may cause image quality degradation for some cells due to aggressive reduction of V_{DD} in order to maximize power savings. In this paper, we maintain the maximum acceptable level of image distortion for human perception while applying OLED-DVS.

B. Zoned OLED display panel

As the OLED panel size has continuously increased, the non-uniform light distribution has become a critical problem for the large-area OLED panel [1]. Although a few solutions have enhanced the luminance uniformity of the OLED panel [2], their efficacy is limited to the relatively small panel size (e.g., 150x150mm^2). This is because the increasing driving current in a large-area panel (e.g., 65" TV panel with 1500x900mm^2 area) induces significant IR-drop through current conducting paths from the power supply to OLED cells. To overcome this problem, researchers have proposed to divide the panel into multiple sub-panels/zones, whereby the sub-panel have different voltage levels compensating their own amounts of IR-drop [12]. For example, if we assume a copper wire of 0.129 mm^2 cross-sectional area (its unit-length resistance is 5.97E-4Ω/mm), used in commercial OLED panels [15], and assuming a 65" 4K panel is divided into 2x2, the resulting IR-drops of the sub-panels can reach a maximum of 6V. Since the typical input voltage level of the OLED panel is around 14$\sim$15V, the 6V IR-drop can cause severe image distortion.

Meanwhile, regardless of the IR-drop issue, the zone-specific OLED-DVS in [3][10][9] also exploits panel partitioning.

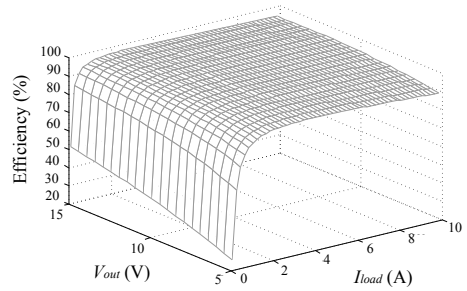

Fig. 1. Buck boost converter. (a) the converter schematic and (b) the conversion efficiency vs. I_{load} and V_{out}.

With minimum image distortion, this method has proved that controlling the sub-panels at finer-granularity can enhance the power efficiency of the OLED panel. However, controlling each sub-panel individually as suggested in [12][3][10] necessitates a dedicated converter for each sub-panel, which incurs significant area overhead and extra cost and may result in low conversion efficiency in the converters. Note that the purpose of the present paper is to show how to design and utilize a configurable switch network comprised of DC-DC converters and powerFETs that will reduce the overhead of the zoned OLED display panels. This paper does not deal with issues having to do with the DVS strategy that is being employed. For example, questions such as how to address any image brightness discontinuity at the boundary between two zones operating at different V_{DD}'s falls outside the scope of the present paper. References [3][10][9] have indeed shown that it is possible to develop a highly effective zone-specific DVS strategy that achieves power savings while maintaining the image quality in large OLED display panels.

C. DC-DC converter characteristics

A converter in an OLED platform that regulates the output voltage V_{out} from $V_{DD} = 12V$ should support both buck-mode control ($V_{out} < V_{DD} = 12V$) and boost-mode control ($V_{out} > V_{DD}$). This buck-boost converter consists of four powerFETs, one inductor, one capacitor and two PWM controllers. Details of the schematic of the buck-boost converter are well described in [16], we thus omit the detailed explanation in this paper.

State-of-the-art converters exhibit high peak power efficiency when the load current is within a certain desirable range, but their efficiency drops significantly when the load current is out of the range. The power conversion efficiency η is defined as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{DD} \cdot I_{load} - P_{DC}}{V_{DD} \cdot I_{load}}, \quad (1)$$

where I_{load} is the load current of the converter, and P_{DC} is the power loss of the converter. We use analytical models presented in [16][14] to derive the P_{DC}. Fig. 1 shows the conversion efficiency as a function of I_{load} and V_{out}. As seen in the figure, the conversion efficiency under small load currents is very low due to the static power consumption of the converter. When the load current is high, the current-induced IR loss will dominate the converter power loss. On the other hand, the output voltage affects the duty ratio of the PWM control and, in turn degrades the efficiency as the difference between the input and output voltages increases.

III. Design and Control of PDN for OLED displays

To maintain image quality, large OLED panels must be divided into multiple sub-panels to maintain the amount of IR-drop below a critical level. However, the optimal design and control of power delivery network (PDN), which comprises of multiple converters connecting from the power source to sub-panels, becomes a critical task that requires investigation. For example, if a 65" OLED panel is divided into 8x8 sub-panels, the methods proposed in [3][10][9] that supply every sub-panel with a dedicated converter will result in 64 converters. These converters may require more than $1000 additional cost and 110 cm^2 space, which is a significant overhead. Moreover, as discussed in Section II-C, the power conversion efficiency of

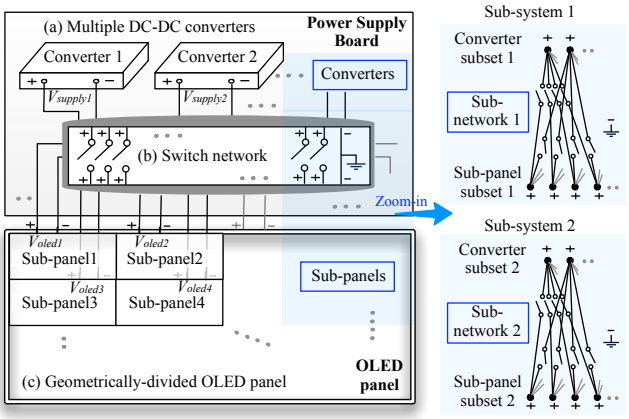

Fig. 2. Geometrically divided OLED display panel with multiple converters connected by the switch network. The switch network is partitioned to sub-networks.

converters drops significantly under adverse load current conditions, which needs to be taken into account in the PDN design and control framework.

In this section, we first explore recent works on PDN architectures and PDN-aware power management. Then we will present the proposed optimal design and control framework of reconfigurable PDN for large-area OLED panels, in order for power consumption minimization accounting for converter characteristics and subject to the IR-drop constraint.

A. PDN architectures in Multicore platform

The problem of minimizing the power consumption of DVS-enabled OLED displays is similar to the power minimization problem using dynamic voltage and frequency scaling (DVFS) in multicore platforms (with/without consideration of the PDN). Therefore, we first explore the previous work on DVFS for multicore platforms. For multicore platforms, per-core DVFS has been proposed to achieve the full potential of power saving by DVFS [17]. This approach faces the problem of high converter overhead because one dedicated converter is required for each core, similarly to the case of applying dedicated DVS to each sub-panel/zone separately in an OLED panel. To tackle this drawback, a per-cluster DVFS method has been suggested [13]. With a new structure of multicore platform that includes clustered cores and converters dedicated to each cluster, this method uses task scheduling and migration schemes (This means, for the target tasks, we select the cores such that cores in each cluster have similar DVFS (i.e., voltage and frequency) levels.) However, in the OLED platform, it is fundamentally impossible to perform such task assignment schemes. Thus we cannot apply this method in the OLED display platform.

Recently, reconfigurable PDNs for the multicore platforms have been presented in [14]. With a reconfigurable switch network and a methodology for converter consolidation, reference [14] supports per-core DVFS and simultaneously achieves high power conversion efficiency. More precisely, the main idea is to combine a certain number of cores, which require relatively small amount of load currents, to be powered by a single converter. As a result, a single converter supplies a relatively high load current likely to be within the high-efficiency range (c.f. Fig. 1), whereas the other converters that are not used can be turned off to save power. Motivated by this work, we propose a reconfigurable PDN for the zoned, large-area OLED panel.

B. Reconfigurable PDN for OLED displays

Motivated by the PDN architectures in multicore platforms, we propose a reconfigurable PDN for a large-area OLED panel. Our presented reconfigurable PDN aims to make a single converter supply power for multiple sub-panels, thereby simultaneously reducing the number of required converters and enhancing power conversion efficiency. More specifically, we adaptively group a number of sub-panels, where each group of sub-panels is connected to a single converter through a switchable network. Although both of our proposed reconfigurable PDN and the one in the multicore platform [14] exploit the benefit from converter consolidation, they have inherent differences: i) the number of converters equipped in the OLED display is less than the total number of sub-panels, thus the sub-panels need to be grouped, ii) grouping the sub-panels and selecting the corresponding converter affect the IR-drop of conducting wires as well as power conversion efficiency, a phenomenon that must be taken into account, and iii) when considering the area overhead of converters and switch network, powerFET switches should be adopted instead of MOSFET switches. This is because the MOSFET switches used in [14] can not drive high current. Hence, we have to use powerFET switches with larger footprint and also higher current driving capability for the OLED panel.

TABLE I
COMPONENT IN A CONVERTER/SWITCH NETWORK.

Component	Spec.	Product	Manufacturer	Price
Inductor	10uH	7447709100	Wurth Electronics	$3.1
Capacitor	10uF	1EA100WR	Panasonic	$0.5
Regulator	Buck-boost	LT3791	Linear Technology	$11.8
PowerFET	N-type	Si1470DH	Vishay Siliconix	$0.8

Fig. 2 shows the proposed reconfigurable PDN architecture for the zoned, large-area OLED display. It consists of a power supply board and an OLED panel. The power supply board includes multiple converters and a switch network, and the OLED panel is divided into multiple sub-panels. Note that we integrate the switch network with the power supply board, because the large footprint of the multiple powerFET switches in the switch network makes it impossible for these switches to be integrated in the future flexible and transparent OLED panels. Using this switch network incurs cost and area overhead. Multiple powerFETs in the switch network, which enable each converter to power multiple sub-panels, induces additional cost and space requirement. However, compared with incorporating additional converters as discussed in [3][10][9], the switch network is more economical. Table I shows an example of component prices for a converter or switch network targeting the application of a 65" OLED panel. We choose LT3791, a buck-boost LED driver controller, along with one inductor, three capacitors and four powerFETs to build one converter, which costs around $19.6. Notice that with this same dollar amount, one can purchase and use roughly 24 powerFETs in the switch network. In addition, the converter occupies at least 172mm^2 printed circuit board (PCB) area, while a single powerFET switch occupies only around 4mm^2.

The switch network in Fig. 2 makes it possible to minimize the power loss of the multiple converters. For example, let us assume there are 8 sub-panels, each of which requires less than 100mA (i.e., the luminance of pixels in these sub-panels may be very low). If each converter is dedicated to each sub-panel, the conversion efficiency may be less than 50% (cf. Fig. 1). However, if we configure the switch network to connect a single converter to the 8 sub-panels, the single converter drives 800mA, thus achieves more than 75% efficiency. To do so, because of single output voltage level of a converter, the voltage levels of the sub-panels should be the same. This constraint implies that configuring the switch network is ultimately related to determining the voltage levels of sub-panels. We will discuss this issue in detail at the following subsection.

Although the switch network has advantages in terms of conversion efficiency and area/cost overhead of the multiple converters, the complexity of switch network needs to be controlled, and therefore the number of sub-panels that one converter can be connected to should be limited. For each converter, the required number of powerFET switches linearly increases with the number of sub-panels. Namely, to support one converter to connect to all sub-panels of an A *by* B array, $A \cdot B$ switches are needed. If A and B values are large, the area/cost overhead of switches becomes significant. Moreover, using too many switches gives rise to wasted power increase from the unused (turned-off) switches. More specifically, the power loss of a powerFET switch P_{SW} is presented in [18][19].

Therefore, we propose that the switch network should be divided into sub-networks, and each converter (and sub-panel) exclusively belong to its own sub-network. In this case, one converter can be connected to all sub-panels belonging to the

same sub-network, i.e., converters and sub-panels that belong to the same sub-network can form a complete bipartite graph (cf. Fig. 2). Of course, at the design time to determine the sub-network size, designers should consider (i) the aforesaid area/cost overhead of powerFET switches, (ii) the maximum current that a single converter will inject into the sub-network, and (iii) the power conversion efficiencies of converters as discussed in Section II-C. A sub-network should be designed to be neither too large due to the requirement of a large number of powerFET switches, nor too small due to the limited freedom in reconfiguration and the low conversion efficiency under low load current conditions. In this paper, we investigate various sizes of sub-networks with 4 by 4 and 8 by 8 divisions of the 65" panel. Details are described at Section IV-B.

C. Dynamic Reconfiguration Algorithm of the PDN

Now we focus on the dynamic reconfiguration of a switch sub-network, which aims to find the group of sub-panels to be powered by each single converter. Assume that the sub-network is connected with N converters and M sub-panels. We aim to find N mutually exclusive groups for all the N converters, where each group corresponds to the set of sub-panels that a single converter drives. This is a partitioning problem with the objective to minimize the overall power consumption of the sub-system including power consumption of sub-panels and power losses of converters, powerFET switches and conducting wires, while maintaining the image quality (with the minimum image distortion).

We first discuss the constraint to maintain the image quality. For the m^{th} sub-panel ($1 \le m \le M$), let $V_{DVS,m}$ denote the minimum supply voltage level on that panel that guarantees the image quality with the minimum distortion as derived in [3][10][9]. We need to account for IR-drop on the wire and powerFET switch, $V_{IR,m}$, which was neglected in [3][10][9], and define $V_{O,m} = V_{DVS,m} + V_{IR,m}$. If the m^{th} sub-panel is connected to the n^{th} converter though the sub-network (i.e., the m^{th} sub-panel belongs to the n^{th} group, $m \in G_n$), then the output voltage of the n^{th} converter, $V_{G,n}$, must satisfy $V_{G,n} \ge V_{O,m}$. In other words, the output voltage $V_{G,n}$ should be the maximum of $V_{O,m}$ values of all sub-panels that are connected to the n^{th} converter, i.e., in the n^{th} group. In this way the image quality with the minimum distortion can be maintained during sub-panel grouping.

We formally describe the problem to find the optimal network configuration to minimize the total power consumption of the sub-system, as follows:

Find N groups G_1, G_2,..., G_N, which are mutually exclusive.

$$\textbf{Minimize} \sum_{n=1}^{N} \left(I_{G,n} \cdot V_{G,n} + P_{DC}(I_{G,n}, V_{G,n})\right).$$

$$\textbf{Subject to } I_{G,n} \le Cap_n,$$

$$\sum_{n=1}^{N} I_{G,n} \cdot V_{G,n} = \sum_{n=1}^{N} \sum_{m \in G_n} P_{panel,m} + P_{network} \qquad (2)$$

In (2), $I_{G,n} = \sum_{m \in G_n} I_m$ and $V_{G,n} = \max_{m \in G_n}(V_{O,m})$ are the output current and voltage of n^{th} converter, where I_m is the driving current of m^{th} sub-panel; P_{DC} is the converter power loss from analytical models presented in [16][14]; $P_{panel,m}$ is the power consumption of m^{th} sub-panel (cf. Section II-A), and $P_{network}$ is the power loss of powerFET switches and conducting wires. Regardless of the grouping results, $P_{network}$ is determined by sub-panels in the sub-system, which can be expressed as:

$$P_{network} = \sum_{m=1}^{M} \left(P_{SW}(I_m) + I_m^2 \cdot R_{wire,m}\right), \qquad (3)$$

where P_{SW} is the switch power loss, which is a function of I_m, and the second term is the conduction loss of the wire.

Algorithm: PDNC - PDN Configuration algorithm

```
Data: I_1,...I_M, and V_O,1,...V_O,M.
Initialization
 Based on V_O of each sub panel, partition the M sub-panels to
 the N groups by using K-means clustering.
 Update V_G,n = max_{m∈G_n}(V_O,m).
// Because V_G,n ≥ V_O,m, pre-specified image distortion thresholds should not be exceeded.
 Arrange G_n so that V_G,n < V_G,n+1 for 1 ≤ n ≤ N−1
 Global variable c=Σ_{n=1}^{N} (I_G,n · V_G,n + P_DC(I_G,n, V_G,n))
Function isGain (I_G,1,...,I_G,N, V_G,1,...,V_G,N) = 0)
    if c≥Σ_{n=1}^{N} (I_G,n · V_G,n + P_DC(I_G,n, V_G,n)) then
        c ← Σ_{n=1}^{N} (I_G,n · V_G,n + P_DC(I_G,n, V_G,n)) return= 1
    end
    return= 0
end
Function Optimization ()                                   // Main function
    Define I_n,m: I_m if m ∈ G_n.
    for 1 ≤ n ≤ N−1 do
        while G_n+1 ≠ ϕ & I_G,n ≤ Cap_n do
            Find m such that I_m = min(I_n+1,m∈G_n+1).
            Move m from G_n+1 to G_n.
            I_G,n ← I_G,n + I_m; V_G,n ← V_G,n+1; I_G,n+1 ← I_G,n+1 − I_m;
            if isGain(I_G,1,...,I_G,N, V_G,1,...,V_G,N) = 0 then
                break
            end
        end
        if G_n+1 = ϕ then G_n+1 ← G_n
    end
```

$R_{wire,m}$ is the resistance of the wire that connects m^{th} sub-panel and the power supply board. In (2), Cap_n is the current driving capability of n^{th} converter that is generally provided by controller data sheets.

The problem is NP-hard. To prove the NP hardness of the problem, we note that the problem difficulty can be reduced by assuming that the resulting power consumption from assigning a specific sub-panel to each converter is pre-determined and independent of other sub-panel assignments. Now the problem becomes a *generalized assignment problem*, which is a well-known NP-hard problem.

To solve the original problem, we propose a clustering-based heuristic algorithm called PDNC. At the initialization procedure, we set the all (N) converters to be utilized to power all (M) sub-panels. Namely, M sub-panels are partitioned into the N groups. Because the voltage level of the grouped sub-panels is adjusted to be $\max_{m \in G_n}(V_{O,m})$, the grouping may increase the power consumption of some sub-panels whose voltage level became higher. In order to minimize this appreciable power loss from the grouping, we propose to use the *k-means clustering* method. The grouping is performed based on V_O values, so that the total intra-group distances of the V_O's within a cluster are minimized and the total inter-group distances of the V_O's across different groups are maximized. Then, we pay attention to the power loss of the converters. The converter efficiency depends on the output voltage and load current of the converter, and it may be quite low if the output voltage or load current is low. We exploit the OLED characteristics that the voltage level of the OLED cell directly affects its driving current. Namely, the sub-panel groups that have low $mean(V_O's)$ values are likely to have small driving current. Hence, we process the groups in ascending order of their voltage level. To do so, we arrange the groups in a way that $G_n : V_{G,n} < V_{G,n+1}$, and start processing from $n = 1$ to $n = N-1$. We first move an element (sub-panel) in G_2, which has the minimum current value $I_{2,1}$ (i.e., we define $I_{n,m}$: I_m if $m \in G_n$, in the PDNC algorithm), to G_1. The results is $V_{G,1} = V_{G,2}$ and $I_{G,1} = I_{G,1} + I_{2,1}$. Next, we check whether this move decreases total power consumption or not. If so, we keep repeating the move until there is no more power saving or the driving current exceeds the maximum capability of a converter. During the procedure, if all the elements in $G_{x>n}$ are moved to G_n, we replace G_x with G_n. Every single replacement turns off one converter (i.e., we can also save power by turning off the converters). In Algorithm 1, the main function *Optimization* performs the aforementioned procedure.

The proposed reconfigurable architecture relies on a dedicated controller to calculate the clustered voltage levels for

(a) Original 4K images (`Balloons', `Bridge', `Colosseum', and `Heidelberg')

10.05V 7.22W	9.97V 9.10W	8.73V 4.91W	9.01V 5.92W	7.86V 0.77W	7.84V 0.84W	7.95V 1.01W	7.89V 1.08W	9.27V 4.02W	10.98V 22.42W	11.51V 57.33W	12.88V 67.36W	12.89V 71.68W	12.27V 81.41W	12.59V 93.43W	14.02V 98.86W
10.49V 19.02W	10.26V 25.39W	10.09V 18.23W	10.31V 15.00V	8.89V 7.04W	9.46V 9.02W	9.46V 9.11W	8.80V 7.18W	9.66V 7.13W	10.68V 42.71W	11.21V 67.23W	11.48V 43.88W	10.73V 26.71W	11.02V 57.45W	11.65V 89.48W	12.81V 83.62W
9.99V 10.93W	9.92V 23.78W	10.02V 31.16W	10.44V 24.64W	9.93V 17.32W	9.69V 20.84W	9.70V 21.62W	10.06V 18.53W	9.69V 5.07W	9.87V 19.61W	10.02V 31.28W	9.99V 10.93W	8.92V 3.14W	9.30V 7.05W	9.85V 18.08W	10.14V 18.08W
9.70V 4.43W	9.60V 12.82W	9.60V 18.85W	9.86V 11.62W	9.51V 8.92W	9.40V 13.64W	9.40V 12.66W	9.56V 11.28W	9.27V 2.95W	9.50V 18.18W	9.50V 10.43W	9.68V 3.60W	8.81V 4.48W	8.50V 2.51W	8.80V 3.58V	9.06V 6.29W

(b) DVS results (voltage level ($V_O = V_{DVS} + V_{IR}$) and power consumption)

Fig. 3. Examples of applying OLED-DVS to 4K images in a 4x4 zoned 65" OLED display panel. The red (blue) box indicate an extreme case of a sub-panel with low (high) luminance pixels.

zones and to issue voltage setting commands to each zone. The controller is in turn implemented as code running on a standard low-power microprocessor (this is a similar architecture as that presented in reference [14]). For video streaming applications whose frame rates are 30 (or 60) fps, reference [9] has reported that the time overhead of OLED-DVS is less than 10% of the frame processing time, and therefore, performing DVS does not affect the image quality. Because the number of clusters (N, which is the number of converters) and the number of entities to be clustered (M, which is the number of sub-panels) per sub-network is rather small (i.e., maximum 5 converters and 16 sub-panels in our experimental work), the runtime overhead of our k-means clustering based algorithm is quite short (i.e., its complexity is $O(MN)$ if Lloyd's algorithm is used in K-mean clustering). Also the delay of reconfiguring the switch network is very short (the maximum delay of the powerFET switch, Si1470DH, is 129.65ns). Therefore, the runtime overhead of our proposed method is quite small. Same applies to the power overhead. As considering the amount of power saving that our reconfigurable network provides, the power overhead of the network itself is very small. For example, if there are 8 sub-panels and 4 converters in a sub-network, each of which sub-panel requires 1A with 12V, the power overhead of the required 32 powerFET switches (Si1470D) should be ~2.1W, which is only 2.2% of the energy consumption of the 8 sub-panels. Therefore, our method will be applicable to video streaming applications with very little delay or power impacts.

IV. Experimental Validation

A. Simulation Framework

We use a pixel-level power model to estimate the power consumption of the OLED panel. Based on the opto-electric efficiency, different color pixels consumes different amount of power. Specifically, the blue pixels are usually implemented in larger size, and consume almost twice power compared to the other colors. Also the power dissipated in the parasitic resistance of the cells depends on the supply voltage of the driver circuit for DVS. The pixel-level power model introduced in [8] captures such color and supply voltage dependencies of the OLED power consumption. The pixel power consumptions are aggregated to estimated the panel power consumption.

To evaluate the image distortion, we use CIELAB color space that is designed to approximate the human visual perception. Based on the measured current of each RGB cell, we perform the regression analysis, so that we first translate the pixel color in CIEXYZ color. Then we transform the XYZ to the Lab color space, by using the transform function [20]:

$$L = 116 \cdot f(Y/Y_w) - 16, a = 500 \cdot f(X/X_w) - f(Y/Y_w)$$
$$b = 200 \cdot f(Y/Y_w) - f(Z/Z_w), \text{ where } f(t) = t^{\frac{1}{3}}. \quad (4)$$

In (4), L, a, and b represent the lightness of the color, red-green content, and yellow-blue content, respectively; X_w, Y_w and Z_w are the color coordinate values of reference white color. We use the Euclidean distance in the Lab color space as a metric to measure the color difference, e_{pixel}, between the original color (L_o, a_o, b_o) and changed color (L_c, a_c, b_c) of the pixel. Details to calculate e_{pixel} is presented in [8]. The image distortion ratio, e_{image}, is $\frac{\text{Number of pixels such that } e_{pixel} > 0.05}{\text{Total number of pixels}} \cdot 100\ (\%)$.

Fig. 3 shows some examples when we apply the OLED-DVS to the 65" OLED panel. We set $e_{image} = 5\%$, and use four 4K images namely 'Balloons', 'Bridge', 'Colosseum' and 'Heidelberg'. The target panel is divided to 4 by 4, thus a total of 16 sub-panels. The derived voltage level of each panel ($V_{O,m} = V_{DVS,m} + V_{IR,m}$) is listed in the figure. To derive the wire resistance, we use a copper wire of 0.129 mm^2 cross-section. As seen in the figure, if a sub-panel mainly consists of the pixels with low brightness (e.g., indicated by red box), its V_O is relatively small, likely because i) DVS may be so effective, and ii) the small I_{panel} may cause small amount of IR-drop. The opposite case of a sub-panel with high brightness (e.g., indicated by blue box in the figure) shows that its V_O is relatively high. This is because the DVS was not so effective or there was significant IR-drop.

Meanwhile, we use an analytical model introduced in [16] to estimate the power loss of the converter. LT3791 buck-boost controller is used with four powerFETs, 10uH inductor, 30uF capacitor, which are in Table I. Fig. 1 illustrates the resulted efficiency of the converter: we change the V_{DD} from 5V to 15V, and I_{load} from 0A to 5A. The figure shows that small load currents and low output voltages result in the low efficiency. For example, in Fig. 3, the sub-panels in the red box, which drive ~100mA with ~8V, have less than 70% converter efficiency, while the sub-panels in the blue box have over 90% converter efficiency.

B. Simulation results

We first investigate a case that the panel is divided by 4x4 (i.e., thus we have total 16 sub-panels, as seen in Fig. 3.) We then determine three different sub-network setups, each of which delivering power to the (upper or lower) 8 sub-panels from 4, 3 and 2 converters. According to the number of converters and sub-panels in a sub-network, we notate the proposed methods: *DVS 8:4*, *8:3*, and *8:2* imply that there are 8 sub-panels with 4, 3 and 2 converters in a sub-network. Table II shows the simulation results for 5 different methods including i) DVS is applied to whole panel [8] (denoted by *DVS 16:1*), ii) DVS is applied to each sub-panel [3][10][9] (denoted by *DVS 16:16*), and proposed methods. As a reference point, *DVS NO* column lists the power consumption values for cases without any DVS. For the results of the proposed methods, the power consumption of the powerFET switches (Si1470D) are calculated and included in Table II. Meanwhile, to estimate the cost for each method, we used the price information of each component in a converter, shown at

TABLE II

SIMULATION RESULTS OF A 65" 4K OLED PANEL DIVIDED BY 4X4: $P_{DVS,\ n:m}$'S DENOTE THE POWER CONSUMPTION OF THE PANEL, CONVERTER(S) AND SWITCH NETWORK WHEN DVS IS APPLIED TO n SUB-PANELS WITH m CONVERTERS. *NO* MEANS NO DVS APPLIED, *DVS 16:1* APPLIES DVS TO WHOLE PANEL [8], *DVS 16:16* APPLIES DVS TO EACH SUB-PANEL [3], [10], [9], AND *DVS 8:4*, *DVS 8:3* AND *DVS 8:2* PERFORM DVS WITH RECONFIGURABLE PDNS (SUB- PANELS ARE GROUPED TO 2 SUB-NETWORKS, EACH OF WHICH HAS THUS 8 SUB-PANELS.) POWER SAVING (%) FOR EACH METHOD IS PROVIDED. ADDITIONAL IMPLEMENTATION COSTS ARE ALSO PROVIDED (DETAILS TO CALCULATE THE ADD. COST ARE DESCRIBED IN SECTION IV-B.)

Image	No DVS	Previously presented methods		Our proposed methods		
	$P_{DVS\ NO}$ (W)	$P_{DVS\ 16:1}$ [8] (W)	$P_{DVS\ 16:16}$ [3], [10], [9] (W)	$P_{DVS\ 8:4}$ (W)	$P_{DVS\ 8:3}$ (W)	$P_{DVS\ 8:2}$ (W)
'Balloons'	395.2	285.6 (27.7%)	256.8 (35.0%)	255.2 (35.4%)	258.9 (34.5%)	261.7 (33.7%)
'Bridge'	268.4	184.8 (31%)	173.6 (35.3%)	169.5 (36.8%)	170.4 (36.5%)	172.2 (35.8%)
'Colosseum'	641.4	570.5 (11.1%)	433.1 (32.5%)	439.8 (31.4%)	448.11 (30.1%)	471.5 (26.5%)
'Heidelberg'	985.9	977.9 (0.8%)	696.3 (29.4%)	730.5 (25.9%)	751.1 (23.8%)	799.4 (18.9%)
Additional cost		–	$\sim$294	$\sim$188.4	$\sim$136.4	$\sim$84.4

TABLE III

SIMULATION RESULTS OF 8X8 PANEL DIVISION: P_{method}'S FOLLOW THE SAME NOTATION IN TABLE III. $P_{DVS\ 64:64}$ IS FROM [3], [10], [9], AND $P_{DVS\ 16:5}$ AND $P_{DVS\ 16:2}$ ARE FROM OUR PROPOSED METHODS.

Image	$P_{DVS\ 64:64}$ (W)	$P_{DVS\ 16:5}$ (W)	$P_{DVS\ 16:2}$ (W)
'Balloons'	281.4 (25%)	252.3 (32.8%)	249.4 (33.5%)
'Bridge'	201.8 (22.5%)	172.2 (33.91%)	168.2 (35.5%)
'Colosseum'	423.9 (28.9%)	399.6 (33.0%)	402.95 (32.5%)
'Heidelberg'	618.4 (30.9%)	602.8 (32.7%)	626.5 (30.1%)
Add. cost	$\sim$1254.4	$\sim$648	$\sim$259.2

Table 1. For example, as one converter costs $19.6 (one buck-boost LED driver controller, one inductor, three capacitors and four powerFETs, as previously mentioned in Section III-C), *DVS 16:16*, which requires additional 15 converters, results in an additional cost of $294 whereas *DVS* $8:4$ requires only additional 7 converters and 64 powerFET switches with a total cost of $188.4. Similarly, the additional cost for the other methods are calculated.

As expected, *DVS 16:16* saves more amount of power than *DVS 16:1*. Esp., *DVS 16:16* achieves remarkable power saving with 'Colosseum' and 'Heidelberg', which consume high power with the highest luminance pixels (cf. blue box in Fig. 3). However, implementing *DVS 16:16* costs extra $\sim$294, which is expensive. On the other hands, compared to *DVS 16:16*, the results of the proposed methods show that they can achieve similar power saving levels by much less expenses. Furthermore, if images do not require many number of pixels to have high luminance, the proposed methods can save more power than *DVS 16:16* does. For example, *DVS 8:4* saves 37% power in 'Bridge', but *DVS 16:16* saves 35% power. This is thanks to one of the benefits of the proposed reconfigurable PDN, i.e, fewer number of converters, which lowers power consumption. Moreover, each converter may have higher efficiency than the converter used in *DVS 16:16*. Also note that the cost of implementing *DVS 8:4* is 36% lower than that of *DVS 16:16*.

Next, we divide the panel to 8x8, hence we have finer-grained 64 sub-panels. Corresponding results are shown in Table III. Table III shows that compared to our proposed methods, *DVS 64:64* saves a little more power in 'Colosseum' and 'Heidelberg', owing to the benefit of fine granularity control. However the high number of converters in *DVS 64:64* makes it very costly. E.g., our proposed *DVS 16:2* costs 5 times as low as that of *DVS 64:64*, with similar or lower power saving achievements. In another example, *DVS 8:2* (in Table II: costs less than a $100) results in higher power savings than *DVS 64:64* (which costs a $1000 more for some low luminance images.)

The results in Table II and III confirm that the proposed framework consistently achieves high power conversion efficiency and significant energy saving while minimizing the overheads of the converters.

V. CONCLUSION

Recently, a dynamic supply voltage scaling of OLED display (OLED-DVS) was introduced, in order to reduce the power consumption of the OLED panels only with negligible displayed image distortion. Application of the OLED-DVS with zoned control was also investigated. However, there has been no dedicated work for the design of PDN to realize the OLED-DVS on large-area display. In this paper, we introduce a reconfigurable PDN architecture and its optimization control to realize the OLED-DVS on large-area display. The large-area OLED panel is partitioned into multiple sub-panels for each of which the supply voltage is adaptively adjusted based on the displayed content. The proposed PDN architecture consists of limited number of converters and switch networks to supply the required voltage in time. The proposed framework minimizes the overhead of the multiple converters, and consistently achieves high power conversion efficiency and significant energy saving while satisfying the IR drop constraint. The experimental results confirm that the proposed method achieves up to 36% power savings in a 65" 4K OLED display platform.

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