Probability Calculation of Read Failures in Nano-Scaled SRAM Cells under Process Variations

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***Abstract*—In this paper, we present an accurate method for predicting the read failure probability of SRAM cells. First, using a simple I-V model for transistors, analytical expressions for the V_{read} and V_{trip} of SRAM cells are obtained. These expressions are subsequently used to derive a fairly accurate model for the read margin of SRAM cells. Then, using Jacobian determinant, the joint probability density function for the V_{read} and V_{trip} is calculated without assuming any specific distribution function for its probability. The accuracy of the approach is studied by comparing its results with those of a previous technique and HSPICE-based Monte Carlo simulations for a 32 nm CMOS technology. The study shows that the proposed technique has on average about 31% lower error when compared to the previous approach. In addition to a higher accuracy, the method has the advantage of not being restricted to a specific probability distribution form.**

***Index Terms*— Manufacturing process variation, SRAM cell, read failure probability.**

I. INTRODUCTION

Process variations have had a large impact on performance and functionality of nano-scaled Static Random Access Memory (SRAM) cells. Predicting the statistical distribution of parameters due to process variations is critical in modern digital designs where multi-Gb memories are employed. The requirements for these designs include assuring reliability in a few parts per billion range in the presence of parameter variations [1]. The variations of parameter can be categorized into inter-die versus intra-die variations and further subdivided into systematic and random variations [2]. Inter-die variations, which stem mainly from wafer manufacturing processes, cause the same device to feature different characteristics across different dies. Intra-die variations, which originate from processes like sub-wavelength lithography and random dopant diffusion, are responsible for variations in device characteristics within a single die (chip) [3]. Also, note that intra-die variations of some parameters, which are mainly geometry/layout related parameters, have some spatial correlations while fluctuations of some others parameters, which are process related parameters, exhibit almost no spatial correlation [3]. Examples of the former include channel length/width and oxide thickness while examples of the latter consist of channel dopant concentration and surface roughness.

SRAM cell failures can occur due to an increase in the cell access time (access time failure), unstable read (flipping of the cell data while reading) and/or write problems (inability to successfully write to a cell.) These failures are collectively referred to as read/write failures. SRAM cell failures can also occur due to a failure in the data holding capability of the cell, specially, flipping of the cell data with the application of a supply voltage lower than the nominal one in the standby mode (known as hold failure in the standby mode.) The aforesaid cell failures may be caused by variations in the device parameters, and hence, are commonly called parametric failures [4][5]. The focus of this work is on the read failure.

There are a number of previous works which have concentrated on read failure probability of SRAMs as a result of process variations. Some works like [6] and [7] present only analyses of the read failure rate of SRAMs without attempting to model it. Other work [8] presents a good method for numerical estimation of read failure probability (again without any analytical modeling). There are also some efforts, including [3] and [9], which present modeling techniques to estimate the read failure probability of SRAM. In [9], a technique based on piecewise modeling and controlled sampling is presented. The approach proposed in [3], which only takes into account the threshold voltage variation, views the parameter space as divided into two regions: pass or fail. This classification requires prior circuit simulations by engines like SPICE. In contrast our proposed approach may be easily used for various sources of variation (threshold voltage as well as others.) In addition, our proposed approach relies on a direct model for the read failure probability calculation based on variations of instance parameters, which are circuit parameters explicitly provided in the netlist of SPICE and the associated transistor parameters such as the transistor width, length, oxide thickness and threshold voltage.

A work that directly addresses the read failure probability of SRAM cell is reported in [10]. In this work, the author assumes a Gaussian distribution function for the variation of the target parameter of interest. The analytical models in [10] are, however, based on the square law device current equation which is not valid for sub-45 nm technology.

In this paper, we invoke a general framework for obtaining the read failure probability of the SRAM cells without assuming any specific form for its distribution.

The rest of the paper is organized as follows. In Section II, a transistor *I-V* model and the derivation of the analytical expressions for the SRAM cell V_{read} and V_{trip} based on the model are discussed. Section III presents the suggested approach for calculating the joint probability distribution function of the V_{read} and V_{trip} which results in finding read failure probability. Simulation results are discussed in Section IV whereas Section V concludes the paper.

II. METHODOLOGY

The read failure occurs due to the corruption of the stored data in the cell while accessing it. During the read operation of the cell shown in Fig. 1 (*VL* = "1" and *VR* = "0"), the voltage at node *R* (*VR*) increases to a positive value, denoted by V_{read}, set by the voltage divider formed by the right access transistor (*AR*) and the right pull down transistor (*NR*). If V_{read} is higher than the trip point of the left inverter (*PL* − *NL*), denoted by V_{trip}, then the cell flips and a read failure occurs. In this section, first, we describe a simple transistor *I-V* model whose accuracy is good enough for the voltage ranges of our interest

in this work. Then, the model is used to derive analytical expressions for the cell V_{read} and V_{trip}.

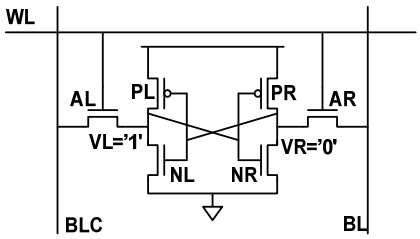

Fig. 1. Conventional 6T SRAM cell (VL = "1" and VR = "0").

A. I-V Model

Modeling V_{read} and V_{trip} of a SRAM cell requires an accurate model for the MOSFET I-V characteristics. There have been many efforts to include second-order effects such as velocity saturation and short-channel effects in nano-scaled regime (see e.g., [11], [12]). Simplicity of the model is critical to obtaining analytical expressions for V_{read} and V_{trip} for sub-45 nm transistors. Thus, one may use simple models with reasonable accuracies such as the n^{th} power model [13]. Here, we also use the n^{th} power model. In this model, the ON current in the saturation (I_{Dsat}) and linear (I_{Dlin}) regions are, respectively, given by [14]

$$I_{\mathrm{Dsat}} = \frac{W}{L_g} B(V_{gs} - V_{th})^n \quad V_{ds} \geq V_{\mathrm{Dsat}} \tag{1}$$

$$I_{\mathrm{Dlin}} = I_{\mathrm{Dsat}}\left(2 - \frac{V_{ds}}{V_{\mathrm{Dsat}}}\right)\frac{V_{ds}}{V_{\mathrm{Dsat}}} \quad V_{ds} < V_{\mathrm{Dsat}} \tag{2}$$

where W is the channel width, L_g is the channel length, and V_{gs} and V_{ds} are the gate-source and drain-source voltages, respectively and

$$V_{\mathrm{Dsat}} = K(V_{gs} - V_{th})^m . \tag{3}$$

For the threshold voltage, we use the short channel model considering DIBL and body effect as [14]

$$V_{th} = V_{th0} + fV_{sb} - V_{ds}\exp\left(-\frac{L_g}{l}\right). \tag{4}$$

In these equations, V_{th0} is the zero body-bias threshold voltage, and m, n, l, f, B, K are fitting parameters which are found by fitting the above equations to the results obtained from the HSPICE simulations or experimental data.

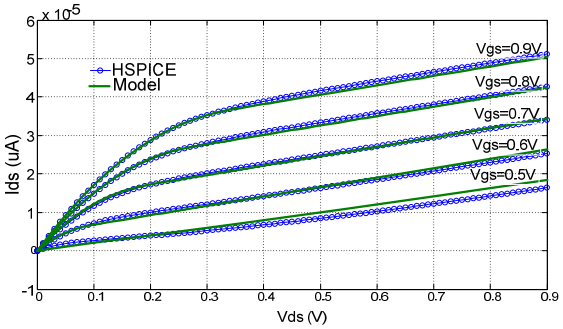

Fig. 2. I_{ds}-V_{ds} characteristic for 32nm technology NMOS using the model and simulations (the width of transistor is 48nm). The fitted value for n was assumed to be almost 1 for NMOS.

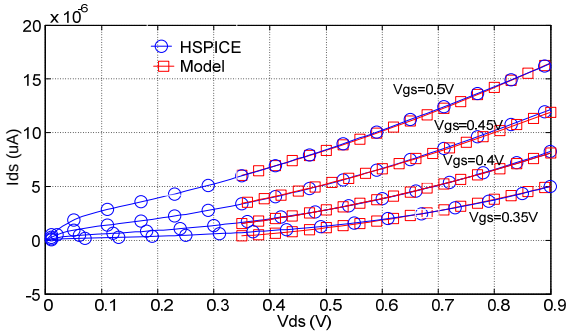

Fig. 3. I_{ds}-V_{ds} characteristic for 32nm technology NMOS using the model and simulations for low V_{gs} (only saturation region has been modeled). The fitted value for n was assumed to be almost 2.

For the PTM 32nm technology [15], the fitted values for n are almost 1 and 1.5 for NMOS and PMOS, respectively. Using these values for n, the other fitting parameters may be easily found from the simulations by using the method of least squares. The results of the model and HSPICE are compared in Fig. 2. The comparison shows that although the model results fit well with the simulation results for high value of V_{gs}, the accuracy is not good enough for low V_{gs} values. For calculating V_{trip}, we need high accuracy at low V_{gs} values. Therefore, making use of the above fitting parameters adversely affects the accuracy.

Our simulations revealed that for low V_{gs} values, if we set n equal to 2 and repeat the fitting procedure, an acceptable accuracy will be obtained for low V_{gs} values as shown in Fig. 3 for an NMOS transistor. A similar result was found for PMOS transistor. This can be explained using the model presented in [14] as follows. Consider the saturation current for short channel devices

$$I_{\mathrm{Dsat}} = \frac{WC_{ox}\mu_{eff}}{2L}\frac{(V_{gs} - V_{th})^2}{1 + \dfrac{V_{gs} - V_{th}}{E_{\mathrm{sat}}L}} \tag{5}$$

Equation (5) shows that for low V_{gs}-V_{th} the second term in the denominator becomes negligible. In other words, the velocity saturation effect may be neglected. Finally, note that although the results presented here are for the 32nm technology node, the same approach may be used for smaller feature size technologies as well.

B. Read Voltage and Trip Voltage Modeling

The read margin defined as $V_{trip} - V_{read}$ is considered as a proper metric for the read stability of SRAM cells [16]. The read margin is positive for a stable read operation. In a conventional 6-transistor SRAM cell as shown in Fig. 1, the V_{read} and V_{trip} can be found analytically from the KCL equations at the storage nodes [10]. For example, V_{trip} can be found by using the KCL equation at node L when VL and VR are set to V_{trip} as follows

$$\begin{aligned} &I_{\mathrm{Dsat-NL}}(V_g = V_{\mathrm{trip}}, V_s = 0, V_d = V_{\mathrm{trip}}) \\ &= I_{\mathrm{Dsat-PL}}(V_g = V_{\mathrm{trip}}, V_s = V_{dd}, V_d = V_{\mathrm{trip}}) \\ &\qquad + I_{\mathrm{Dsat-AL}}(V_g = V_{dd}, V_s = V_{\mathrm{trip}}, V_d = V_{dd}). \end{aligned} \tag{6}$$

Also, V_{read} is found by using the KCL equation at the node R during the read operation assuming VL to be V_{dd} as follows

$$I_{\text{Dsat-AR}}(V_g = V_{dd}, V_s = V_{\text{read}}, V_d = V_{dd}) = I_{\text{Dlin-NR}}(V_g = V_{dd}, V_s = 0, V_d = V_{\text{read}}) . \quad (7)$$

In these equations, the leakage currents have been neglected. Next, we use the analytical model obtained for the *I-V* characteristic of the transistor to derive the expressions for the calculation of V_{read} and V_{trip} of the 6T SRAM cell. Using (1) and (6), V_{trip} can be easily found by solving a second order polynomial equation with respect to V_{trip}. Since the explicit form of the equation is complex, we show the implicit form of this equation which is given by

$$\beta\ B_{nl}(V_{\text{trip}} - (V_{th0-nl} - V_{\text{trip}} \exp(-\frac{L_{NL}}{l_{nl}})))^2 \quad (8)$$
$$= \alpha\ B_{pl}(V_{dd} - V_{\text{trip}} - (-V_{th0-pl} - (V_{dd} - V_{\text{trip}}) \exp(-\frac{L_{PL}}{l_{pl}})))^2$$
$$+ B_{nl}(V_{dd} - V_{\text{trip}} - (V_{th0-nl} + f_{nl} - (V_{dd} - V_{\text{trip}}) \exp(-\frac{L_{AL}}{l_{nl}})))^2 .$$

Here, the subscript *n* and *p* refer to the fitting parameter for NMOS and PMOS, respectively while the subscript *l* indicates the fitting parameters for low V_{gs} values. Also, β denotes the size ratio for the pull down transistors and the access transistors which is given by

$$\beta = \frac{(\frac{W}{L})_{NL-NR}}{(\frac{W}{L})_{AL-AR}} \quad (9)$$

Whereas α is the size ratio for the pull up transistors and the access transistors which is expressed as

$$\alpha = \frac{(\frac{W}{L})_{PL-PR}}{(\frac{W}{L})_{AL-AR}} \quad (10)$$

One can also find an explicit expression for V_{read}. From (3) and (4), we have

$$V_{\text{Dsat-}NR} = K_n(V_{dd} - (V_{th0-n} - V_{\text{read}} \exp(-\frac{L_{NR}}{l_n})))^m \quad (11)$$

Note that the subscript *l* is not present in here which indicates that the fitting parameters are for normal V_{gs} values. Rewriting (11) leads to

$$V_{\text{Dsat-NR}} = K_{\text{n}}(V_{dd} - V_{th0-n})^m (1 + \frac{V_{\text{read}} \exp(-\frac{L_{NR}}{l_n})}{V_{dd} - V_{th0-n}})^m \quad (12)$$

Since the threshold voltage shift of *NR* due to the Drain Induced Barrier Lowering (DIBL) for low V_{ds} values (equal to V_{read}) is very small, we have

$$\frac{V_{\text{read}} \exp(-\frac{L_{NR}}{l_n})}{V_{dd} - V_{th0-n}} << 1 , \quad (13)$$

Hence, one can use the Taylor series expansion to write

$$V_{\text{Dsat-NR}} \cong K_{\text{n}}(V_{\text{dd}} - V_{\text{th0-n}})^m (1 + m\frac{V_{\text{read}} \exp(-\frac{L_{\text{NR}}}{l_{\text{n}}})}{V_{\text{dd}} - V_{\text{th0-n}}}) \quad (14)$$

Using (1), (2), (7), and (14), one can obtain an explicit expression for V_{read} by solving a third order polynomial equation with respect to V_{read}. Again, since the explicit form of the equation for obtaining V_{read} is complex, we present the implicit form of the equation

$$\begin{aligned}
&(V_{dd} - V_{\text{read}} - (V_{th0-n} - (V_{dd} - V_{\text{read}}) \exp(-\frac{L_{AR}}{l_n})))\\
&= \beta\ (V_{dd} - (V_{th0-n} - V_{\text{read}} \exp(\frac{L_{NR}}{l_n})))\\
&\times (2 - \frac{V_{\text{read}}}{V_{\text{read}} \exp(-\frac{L_{NR}}{l_n})})\\
&\qquad K_n(V_{dd} - V_{th0-n})^m (1 - m\frac{V_{dd} - V_{th0-n}}{V_{dd} - V_{th0-n}})\\
&\times \frac{V_{\text{read}}}{V_{\text{read}} \exp(-\frac{L_{NR}}{l_n})}\\
&\qquad K_n(V_{dd} - V_{th0-n})^m (1 - m\frac{V_{dd} - V_{th0-n}}{V_{dd} - V_{th0-n}})
\end{aligned} \quad (15)$$

Finally, the Read Margin (*RM*) can be obtained as

$$RM = V_{\text{trip}} - V_{\text{read}} \quad (16)$$

III. Distribution Function of Read Failure Probability

In order to calculate the read failure rate, the probability that the V_{read} is larger than the V_{trip} of SRAM cell should be calculated. The following expression is the mathematical representation of read failure probability

$$\begin{aligned}
&\textit{Read Failure Probability} = P(RM0 > (V_{\text{trip}} - V_{\text{read}} \equiv RM))\\
&= \int_0^{V_{dd}} \int_0^{V_{\text{read}} + RM0} f_{V_{\text{read}}, V_{\text{trip}}}(V_{\text{read}}, V_{\text{trip}}) . dV_{\text{trip}} . dV_{\text{read}}
\end{aligned} \quad (17)$$

where *RM*0 is the minimum needed read margin. The value of *RM*0 depends on the working environment of the memory cell. In noisy areas this value is larger.

As shown in (17), the calculation of the read failure probability is based on the joint probability density function of the V_{read} and V_{trip}. Having obtained analytical expressions for the voltages, we follow the procedure explained in [17] to calculate the joint density function of these two random variables. Let us assume that the V_{read} and V_{trip} are functions of two independent variables with known joint probability density function as

$$V_{\text{read}} = g(\text{x}, \text{y}) \quad , \quad V_{\text{trip}} = h(\text{x}, \text{y}) \quad (18)$$

where *x* and *y* are random variables (e.g., threshold voltages of two transistors) which are the variation sources in the SRAM cell. The Jacobian function *J*(*x*,*y*) is, by definition, the determinant given by

$$\text{J}(\text{x}, \text{y}) = \begin{vmatrix} \frac{\partial g(x,y)}{\partial x} & \frac{\partial g(x,y)}{\partial y} \\ \frac{\partial h(x,y)}{\partial x} & \frac{\partial h(x,y)}{\partial y} \end{vmatrix} \quad (19)$$

The joint probability density function of the V_{read} and V_{trip} is then expressed as

$$f_{V_{\text{read}},V_{\text{trip}}}(V_{\text{read}},V_{\text{trip}}) = \frac{f_{xy}(x_1,y_1)}{|J(x_1,y_1)|} + \ldots + \frac{f_{xy}(x_i,y_i)}{|J(x_i,y_i)|} \quad (20)$$

where (x_i, y_i) are all pairs satisfying the following equations:

$$g(x_i,y_i)=V_{\text{read}} \ , \quad h(x_i,y_i)=V_{\text{trip}} \quad (21)$$

In this method, the number of independent and dependent variables can be easily extended.

As shown in Fig. 1, assuming that *VR* = "0", transistors *AL*, *AR*, *PL*, *NL*, and *NR* play a role in the read failure analysis. In our case, the threshold voltages of aforementioned transistors are the sources of variation whose associated random variables are, respectively, denoted by x_1 to x_5. Hence, we may write

$$V_{\text{read}} = y_1 = g(x_1,x_2,x_3,x_4,x_5)$$
$$V_{\text{trip}} = y_2 = h(x_1,x_2,x_3,x_4,x_5) \quad (22)$$

In reality, V_{trip} is a function of only x_1, x_3, and x_4 whereas V_{read} is a function of only x_2 and x_5. In order to form a square matrix to calculate the Jacobian function, the numbers of dependant and independent variables should be equal to each other [17]. Hence, we define three auxiliary dependent variables as

$$y_3=x_3 \ , \ y_4=x_4 \ , \ y_5=x_5 \quad (23)$$

For this case, the Jacobian function is obtained from

$$\mathrm{J}(x_1 \ldots x_5) = \begin{vmatrix} 0 & \frac{\partial g}{\partial x_2} & 0 & 0 & \frac{\partial g}{\partial x_5} \\ \frac{\partial h}{\partial x_1} & 0 & \frac{\partial h}{\partial x_3} & \frac{\partial h}{\partial x_4} & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{vmatrix} = \frac{\partial h}{\partial x_1} \times \frac{\partial g}{\partial x_2} \quad (24)$$

IV. Results and Discussion

In this section, the accuracy of the proposed models for calculating V_{read} and V_{trip} is studied. Also, the effectiveness of our proposed methodology for calculating the joint probability density function is compared to that of the work presented [10]. Fig. 4 shows the comparison between V_{trip} and V_{read} of the SRAM cell versus the β ratio for both our proposed model ((5) and (15)) and simulation. This shows a very good accuracy for the model. Next, we discuss the accuracy of the proposed the presence of the process variations. For this study, the 3σ variation for all threshold voltages was assumed to be 20% of the nominal value while considering independent Gaussian distributions for each of them. The frequency plots of V_{read} and V_{trip} of the SRAM cell for 5000 Monte Carlo samples for both model and simulation have been illustrated in Fig. 5.

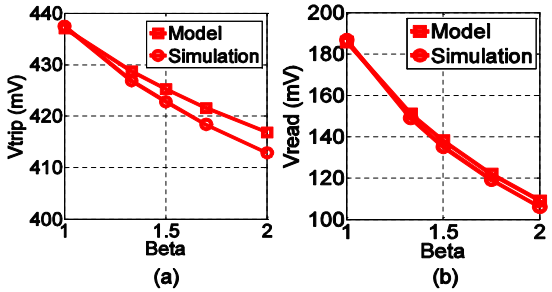

Fig. 4. (a) V_{trip} versus β ratio (b) V_{read} versus β ratio (α ratio is one).

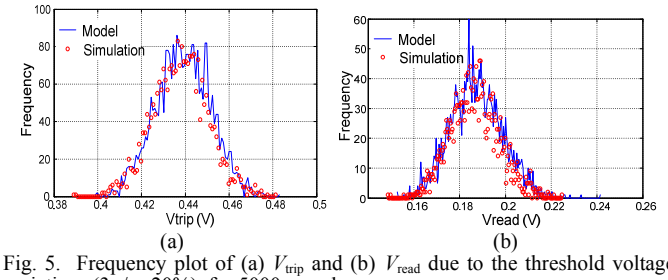

Fig. 5. Frequency plot of (a) V_{trip} and (b) V_{read} due to the threshold voltage variations (3σ/μ=20%) for 5000 samples.

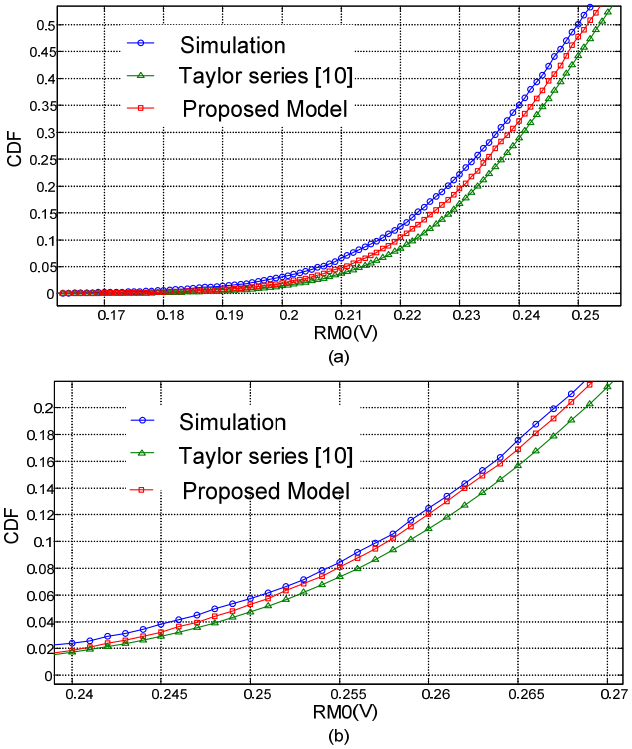

Fig. 6. Cumulative Distribution Function (CDF) of read margin versus minimum needed Read Margin (RM0) due to threshold voltage variation (3σ/μ = 30%) (a) β = 1 (b) β = 1.5.

The statistical information for each histogram is given in Table I which again reveals a high accuracy for the model.

The Cumulative Distribution Function (CDF) of the read margin versus minimum needed read margin is shown in Fig. 6. The CDF value is considered read failure probability for each *RM*0. The read failure modeling in prior work [10] was simply based on the assumption that the read margin as a random variable had a Gaussian distribution. The read margin in [10] was considered as a function of random variables (x_1, x_2, …, x_n) as

$$RM = f(x_1,x_2,\ldots,x_n) \quad (25)$$

TABLE I
Mean Percentage Error (MPE %) of Our Model versus Prior Work [10] due to Variations of Threshold Voltage

	3σ/μ=10%		3σ/μ=20%		3σ/μ=30%	
	β=1	β=1.5	β=1	β=1.5	β=1	β=1.5
Our Model	13.78	11.07	17.71	7.27	22.43	13.44
Prior Work [10]	16.93	21.50	23.74	13.48	33.97	15.23
Improvement	18.60	48.51	25.40	46.07	33.97	11.75

Based on this assumption, the mean and standard deviation of the read margin were obtained through the following Taylor series:

$$\mu_{\mathrm{RM}} = f(\eta_1,...,\eta_n) + \frac{1}{2}\sum_{i=1}^{n}\frac{\partial^2 f}{\partial x_i^2}\Big|_{\eta_i}\sigma_i^2 \quad (26)$$

$$\sigma_{RM}^2 = \sum_{i=1}^{n}\left(\frac{\partial f}{\partial x_i}\Big|_{\eta_i}\right)^2\sigma_i^2 \quad (27)$$

And finally,

Read Failure Probability =

$$P(RM < RM0) = \int_{-\infty}^{RM0}\frac{1}{\sqrt{2\pi}\sigma}e^{-\frac{(RM-\mu_{RM})^2}{2\sigma_{RM}^2}}dRM \quad (28)$$

As discussed previously, our proposed method does not assume any specific statistical distribution for the read margin as a random variable. That is, in our method, variation sources may have any kind of distribution. Using the distribution, the joint probability distribution function of the read and trip voltages is analytically derived. Based on the joint probability distribution function, the read failure probability is modeled.

The accuracies of both techniques versus the simulations are presented in Fig. 6. We performed the simulations for 10, 000 Monte Carlo samples in the 32 nm technology. The comparison reveals a considerably higher accuracy for our proposed technique. The Mean Percentage Errors (MPEs) of both techniques are presented in Table II. The average accuracy improvement achieved by the proposed technique in this work compared to the method suggested in [10] for ($3\sigma/\mu$ = 10-30%) variations of the threshold voltage is 30.7%. The reason that our method is more accurate than the previous work is that no simplifying assumption for the distribution function of the read margin was assumed in this technique. Finally, it should be noted that in using the technique of [10], we used our proposed analytical model for the read margin instead of the simplistic read margin model obtained based on the square law I-V model which gave rise to higher accuracy for the technique of [10].

V. Conclusion

We proposed a methodology for modeling the read failure of SRAM cell under process variations. The proposed method presented a general framework where there was no limitation on the distribution function of the varying parameter of interest. First, a simple yet fairly accurate I-V model was used to derive the read and trip voltages analytically.

TABLE II
MEAN, STANDARD DEVIATION, AND 95TH PERCENTILE OF V_{READ} AND V_{TRIP} WITH PROCESS VARIATIONS OF THRESHOLD VOLTAGE

	V_{trip} (mV)			V_{read} (mV)		
	Model	Simulation	Error (%)	Model	Simulation	Error (%)
Mean	437.2	438.5	0.3	186.2	187.2	0.5
Standard Deviation	12.5	12.7	1.6	10.5	11.5	8.7
95-th Percentile	529.1	526.8	0.4	273.7	277.6	1.4

Then, using a technique based on Jacobian, the joint probability distribution function of read and trip voltage was calculated. Based on this function, the cumulative distribution function of the read margin and consequently the read failure was calculated. The accuracy of the analytical models for the read and trip voltages was shown for a 32 nm technology. Then, the results of the cumulative distribution function for the read margin for both the proposed technique and previous work were compared to the Monte Carlo simulations. The comparison showed that compared to the prior work, the accuracy, on average, improved by about 31% assuming a threshold voltage variations of $3\sigma/\mu$ = 10-30%.

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