Crosstalk Analysis in Nanometer Technologies

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ABSTRACT

Process variations have become a key concern of circuit designers because of their significant, yet hard to predict impact on performance and signal integrity of VLSI circuits. Statistical approaches have been suggested as the most effective substitute for corner-based approaches to deal with the variability of present process technology nodes. This paper introduces a statistical analysis of the crosstalk-aware delay of coupled interconnects considering process variations. The few existing works that have studied this problem suffer not only from shortcomings in their statistical models, but also from inaccurate crosstalk circuit models. We utilize an accurate distributed RC-π model of the interconnections to be able to model process variations close to reality. The considerable effect of correlation among the parameters of neighboring wire segments is also indicated. Statistical properties of the crosstalk-aware output delay are characterized and presented as closed-formed expressions. Monte Carlo Spice-based experimental results demonstrate the effectiveness of the proposed approach in accurately modeling the correlation-aware process variations and their impact on interconnect delay when crosstalk is present.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms

Algorithms, Measurement, Performance, Design, Sensitivity

Keywords

Correlation, crosstalk-aware delay, mean, process variations, statistical static timing analysis, variance, variation shielding

1. INTRODUCTION

The increase in package density as well as the clock frequency of the VLSI circuits has made noise, such as the capacitive coupling noise, one of the most challenging problems in the design and verification of modern VLSI circuits. Furthermore, the interconnect lines get thicker and narrower (and longer in case of global interconnects), which all result in the aggravation of crosstalk noise amplitude and duration, and the circuit faults caused by such noise sources. Therefore as the VLSI technology scales down the role of interconnect parasitic effects in the signal integrity becomes increasingly significant.

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Another unwanted side effect of CMOS process technology scaling is the increase in process variations. Differences between identical features in a certain lithographic process are referred to as *process variations*. Lithography steps generate more process variations in smaller geometric feature sizes. Therefore, cell and interconnect delay characterization methods should consider the increasing impact of process variations on circuit performance and reliability. In addition to IC manufacturing process variations, environmental variations, and device/interconnect aging processes create a rather large deviation of key circuit parameters from their designed values. These phenomena in turn produce timing uncertainty and demand highly sophisticated and robust crosstalk-aware analysis and optimization tools.

The conventional corner-based techniques, to handle variability of parameters will not be effective in nanometer technologies due to their highly pessimistic (and sometimes optimistic) views. Statistical analysis is viewed as an essential methodology for nanometer process technologies, which enables application of the actual statistics of the process technology parameters for the accurate calculation of design characteristics such as delay and noise [1].

Although a great deal of research has been done on statistical static timing analysis, only a few approaches exists in literature that investigate the impact of process variations on crosstalk and inherently circuit performance.

The statistical model of [2] uses a lumped RC model to explore crosstalk-induced pulse (glitch) effect, where a single resistance is extracted to capture the effect of total self resistance of interconnect, regardless of its length. The case for self and coupling capacitances is similar. Also the correlation between the circuit parameters, such as interconnect line resistance and capacitance is assumed to be zero. The statistical model proposed in [3] is more sophisticated and uses a circuit model with higher number of nodes; however, still a single capacitance is extracted to model the total coupling effect, which makes it inappropriate for long interconnect lines. The authors of [4] apply special exponential waveform shapes to analytically study the statistics of crosstalk effect. However the exponential type waveforms cannot accurately represent noise-affected signal waveforms. Additionally, the above approaches are unable to consider the correlation between neighboring wire segments.

The goal of this paper is to study the effect of process variations on some existing crosstalk analysis techniques, resolve their shortcomings, and finally propose an efficient model to statistically calculate the crosstalk-aware delay of the interconnect victim line. More precisely, first a distributed RC-π model is used to accurately capture the statistical variations in the physical dimensions of the interconnect lines and the corresponding electrical parameters. The local effects of process variations on the coupled wire segments and the correlations among variations in neighboring segments are considered in statistical analyses. This information is then used to evaluate the correctness of the existing crosstalk analysis techniques in the presence of process variations using extensive sets of Monte Carlo simulations to

calculate the actual statistical distribution of victim line timing parameters. Finally based on the observations, we propose a set of heuristic solutions for each technique to improve their applicability in statistical analysis of crosstalk effects. This paper is a major extension of our previous work on crosstalk analysis [5] where process variations were ignored.

The remainder of this paper is organized as follows. In section 2 we review the basic aspects of interconnect characterization and modeling considering process variations, their local effects and correlation between parameters. Section 3 explains the experimental setup used for simulation of coupled interconnects in presence of process variations. Sections 4 and 5 summarize the results and conclusions, respectively.

2. INTERCONNECT MODELING

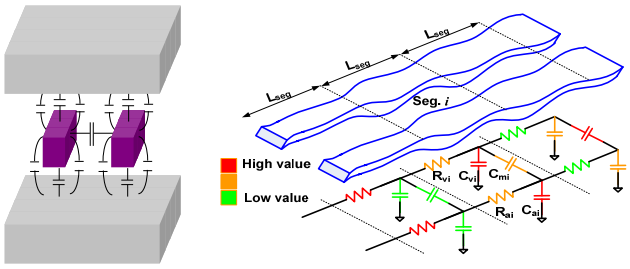
2.1 Crosstalk Terminology

Capacitive coupling between a pair of interconnect lines can induce spurious pulses and/or cause delay effects. We refer to such effects as *crosstalk-induced effects*. The portion of the layout where the coupling occurs is referred to as a *crosstalk site*. Crosstalk-induced slowdown occurs when an *aggressor* line, A, and a *victim* line, V, make signal transitions (state changes) in opposite directions. The net effect, in theory, of the coupling between the two lines is that the transition on the aggressor line tends to slow-down the transition on the victim line, making it appear to be delayed in time. The amount of slow-down is the difference between the time the signal transition at the far-end of the victim line crosses $0.5V_{dd}$ when the aggressor has made a transition in the opposite direction, and that when the aggressor remains quiet.

Slowdown is dependent on the victim and aggressor signal transition times, the skew between their signal arrival times, and the parameter values that are reflected in the capacitive and resistive model components. The uncertainty about the crosstalk-induced delay increase/decrease may be due to variations in any of the above parameters.

2.2 Coupled Interconnect Characterization/Modeling

Consider a pair of coupled interconnect lines in some metal layer, which lies in between two dielectric plates (cf. Figure 1(a) in which one segment of the coupled interconnect is depicted.)



(a) (b)

Figure 1: Distributed capacitive modeling of coupled interconnects.

The two interconnect lines run in parallel and are capacitively coupled. Either line can be considered as a victim, while the other may be treated as the aggressor. The goal is to statistically analyze the slowdown of the victim line due to aggressor line activity. A distributed RC-π model (cf. Figure 1(b)) is used to accurately model the abovementioned interconnect line configuration. In this circuit, each RC-π stage represents an interconnect segment of a predefined length, L_{seg}, which is an important factor when considering spatial correlation among physical parameters as will be explained in section 2.3. The coupling between two interconnect lines along segment i is captured by the coupling capacitance C_{mi}. The self capacitance and resistance of the victim interconnect in segment i are denoted by C_{vi} and R_{vi}, respectively. Note that although lengths of all wire segments are identical, due to process variations, parameter values for each segment are different from those for other segments.

The complexity of distributed RC-π circuit model significantly limits its application in real world designs where millions of interconnect lines and hence crosstalk sites are present. Therefore, circuit designers try to derive the electrical behavior of this complex circuit model by approximating its transfer function using different model order reduction techniques [6]-[7].

Reference [8] analyzes the crosstalk-induced effects by using a simple lumped RC model. In this model, each resistor represents the total resistance of each line, whereas two capacitors capture the total self and coupled capacitances along the length of the interconnect line, respectively. The lumped models are highly inaccurate for global interconnects, especially at high clock frequencies. Closed-form expressions by using 2π and 4π configurations have been developed in [9] and [10], respectively. However, the quality of their analysis and optimization tools degrades when using linear equations to model the nonlinear behavior of the drivers. In [11] distributed RC modeling has been used to obtain quantitative measures of crosstalk-induced pulse peak and width. However, the authors have not considered the case slowdown of the victim's transition, where the aggressor is changing in the opposite direction of the victim.

Generally speaking, the existing models for coupled interconnects tend to be inaccurate when significant process variations exist. On the other hand, the complexity of model order reduction techniques significantly increases when considering process variations [7].

2.3 Interconnect Sources of Variation

The variation of physical parameters, such as width and thickness along interconnect lines is in general due to the imprecision in the IC manufacturing process. This is in turn due to effects of the neighboring interconnect lines, non-uniform metal densities, Non-Linear Resistance (NLR) effect, Selective Process Bias (SPB) [12] effect, and thickness variation due to etching and CMP (Chemical Mechanical Polishing). Other sources of variation are die-to-die, wafer-to-wafer, lot-to-lot, and fab-to-fab variations.

Thickness variation modeling is highly dependent on the accuracy of local wire density calculation [13]. The resultant model is expressed in terms of the size of a *density box* surrounding the critical wire segment. This box typically covers any neighbor wires that can influence the thickness of the critical wire segment. However, wires farther away from the critical wire segment do not contribute to the thickness variation as much as those which are closer. So a weighting function is applied by using a rectangular prism for modeling. The following can be used to compute the effective local density, D_{eff}:

$$D_{eff} = \sum_i d(X_i) \cdot w(X_i) \qquad (2.1)$$

where X_i is the size of the density box of segment i, $w(X_i)$ is its weighting factor, and $d(X_i)$ is the density of the density box of segment i. The number of boxes, i (note that the number of boxed is equal to that of wire segments.) the size of the density box, X_i, and the $w(X_i)$ are derived from silicon measurements by the semiconductor manufacturer's technology development group.

The spatial correlation among the variation of neighboring segments is quite important in the crosstalk-induced delay of the victim interconnect. For example most of the variation resulting from chemical-mechanical polishing (CMP) of the inter-layer dielectric (ILD) is based on systematic spatial effects and vanes within-die [14].

The methodology proposed in this paper uses the spatial information to develop a systematic variation model of the coupled interconnects. The parameters corresponding to every pair of points on the interconnect line are correlated. The correlation relation is a function of distance between those two points. More precisely, for each physical parameter, p_i, (e.g., thickness), the correlation between the parameter values corresponding to two points along the interconnect length at locations x_1 and x_2 is as follows:

$$Corr(p_i(x_1), p_i(x_2)) = e^{-(x_1 - x_2)/L_{seg}} \quad (2.2)$$

where $p_i(x_1)$ and $p_i(x_2)$ are the values of parameter p_i at locations x_1 and x_2 along the interconnect. L_{seg} is a predefined segment length that is assumed to be given to us. It is found by a series of characterization and extraction experiments by the manufacturer.

3. EXPERIMENTAL SETUP

3.1 Statistical Model

To capture the effect of variations of physical parameters such as width, height, and interlayer dielectric thickness on the circuit metrics, the following two-step procedure is used for the calculation of electrical parameters of the distributed circuit model:

- *Physical outline generation*: Complete physical outlines of the coupled interconnect lines is generated in this step, including the information about their width, height, and interlayer dielectric thickness along their length and their correlation as described in section 2.3.
- *RC-π stage parameter calculation*: The generated physical outline of the coupled interconnects is used to calculate the corresponding electrical parameters for each interconnect segment.

The key advantage of the proposed modeling approach is the ability to locally capture the effect of process variations on each interconnect segment. This is done by directly calculating the corresponding values of local resistance and capacitance of the RC-π model based on the exact information about the actual geometry of the interconnect lines in each segment. This is in direct contrast with previous approaches [2]-[4], where a single sample of a given parameter is adopted from the corresponding distribution to extract the electrical parameters of the complete circuit model.

Next, each interconnect line is divided to multiple segments of length, L_{seg}=100μm, and a set of parameters is randomly assigned to that segment based on the assumed distribution. To emulate the variations in the physical outline of the interconnect lines a Gaussian distribution is used for each physical parameter. The choices of distribution type, its characterizing parameters, and the correlations among physical parameters are based on the information made available from the semiconductor manufacturer as described in section 2.3.

In the second step, parameter extraction scheme similar to [15] is used to calculate values of different electrical parameters in the RC-π model. Note that although the approach used for parameter extraction may lack absolute accuracy, it provides the required fidelity with respect to different physical dimensions. Moreover, since all of the experiments use the same extraction method, the presented results only capture the differences in the models, and are not impacted by the accuracy of the extraction procedure.

Figure 2 shows the line resistance and capacitance distribution of a segment of two 100μm-long coupled interconnect lines in metal-4. Note that none of these distributions are Gaussian, since the extraction procedures which transform the physical parameters of interconnect lines to the corresponding electrical parameters are non-linear, and therefore, they tend to result in non-Gaussian distributions for the electrical parameters. This is in contrast with the Gaussian-based assumptions used typically in statistical timing analysis methodologies [12], [16]. The best maximum-likelihood fit for these distributions are lognormal distributions, parameters of which are listed in Table 1 with confidence level of 98%. The corresponding fitted probability distribution functions (pdf) are shown by the red outlines in Figure 2.

It is mentioned in [12] that variations in electrical parameters of interconnect may be approximated as normal distributions with the exception of via and contact resistances which should be approximated as lognormal distributions. The Gaussian distribution assumption in this case is found to have and error of 3.5%.

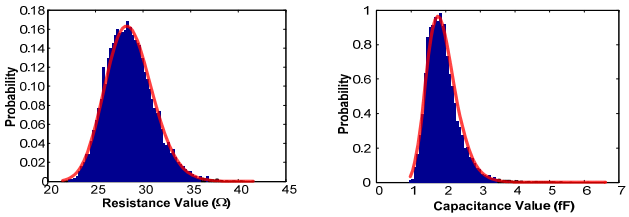


Figure 2: Resistive and Capacitive line distribution for a 0.1mm long metal-4 interconnect

	Resistance (Ω)	Capacitance (pF)
μ	3.3504	0.6271
σ	0.0861	0.2266

Table 1: The mean and standard deviation of the resistance and capacitance line variations depicted in Figure 2.

3.2 The Simulation Setup

To simulate the crosstalk-aware delay of interconnect lines, a distributed circuit consisting of 10 RC-π stages are used (cf. Figure 3.) From now on, we will treat the interconnect with input V_{in} and output V_{out} as the victim line and the other as the aggressor line. The victim and aggressor lines have drivers $Cell_v$ and $Cell_a$ and receivers $4Cell_v$ and $4Cell_a$, respectively. The cells are taken from a standard 130nm, 1.2V production library.

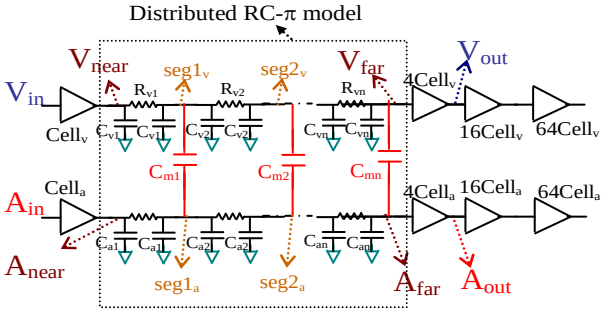


Figure 3: Distributed RC-π modeling of crosstalk site.

To capture the variations of each physical parameter, the two step procedure described in section 3.1 is used to create a large population of samples for each physical parameter which in turn is transformed into the electrical parameters of the distributed RC-π model. Next, Hspice simulation is performed. To achieve convergence in the desired statistical properties of output variables, Monte Carlo simulation is performed. Based on normality assumption for the interconnect delay distribution, a sample size of 2500 is used i.e., the population generation and electrical parameter extraction steps are iterated 2500 times to achieve convergence in the desired statistical properties for each sample. The number of samples is then selected so that a 98% confidence level with 1ps error in the estimates of mean and variance of interconnect delay is achieved.

4. EXPERIMENTAL RESULTS

4.1 Statistical Comparison of Crosstalk Models

To show the necessity of a statistical approach, first the statistical model based on distributed RC-π circuit is compared against the conventional corner-based approach. As seen in Figure 4, the corner-based "μ+3σ" value of the victim delay is equal to 435ps which shows more than 46% pessimism compared to that in our statistical model with distributed circuit modeling (μ+3σ=290).

As discussed earlier, the accuracy of the existing models for coupled interconnects can severely degrade in the existence of process variations. A goal of this work is to investigate the source of inaccuracies for some common crosstalk site models and try to resolve them. The single RC-π model, as well as the 2RC-π model of [17] are considered here as two such models.

The statistical distribution of the delay of the victim line for both approaches is illustrated in Figure 4. The mean delay is found to be very close to the one found by the distributed model (in fact the mean error for the single and two RC-π models is 5% and 3.2%, respectively.) However, the μ+3σ value for the single RC-π and 2RC-π is 330ps and 313ps respectively, meaning there is more than 13% and 7.9% pessimism in μ+3σ calculation when single and 2RC-π are used, respectively. This error mainly exists because when the extraction tool extracts the parameters values for each segment, it extracts the same value for each segment as long as the topology of the wire does not change; subsequently, these identical values are used by a model order reduction technique to create a reduced model such as the lumped RC or RC-π model. However, in reality the local process variations can cause parameter value variations in different segments (cf. section 2.3.)

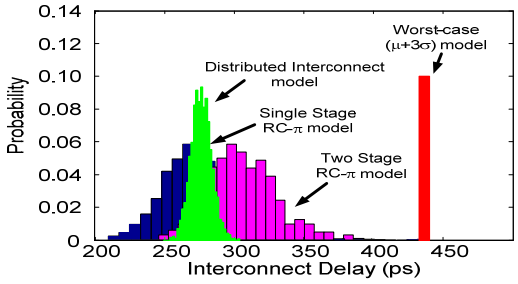


Figure 4: Comparison of different approaches with our statistical crosstalk model

4.2 Variation Shielding

To improve the accuracy of crosstalk models when used in a statistical analysis methodology, we propose the following heuristic algorithm. First, the interconnect line physical parameters are extracted based on conventional scheme. Next before applying the model order reduction formulas to find the capacitive or resistive value of each element in the reduced model with respect to those of each segment of the distributed model, we select the mean and variance of values in each segment as follows. The mean values for all segments are set to the extracted value. The variances are drawn from a family of distributions where their variances decrease geometrically as we proceed towards the far-end of interconnects. The reason behind this type of variance assignment is that based on extensive simulations, we have found that the variation of parameters in each segment is affected by a phenomenon that we refer to as *variation shielding*. By variation shielding, we mean that while moving from an interconnect driver towards the far-end of the interconnect line the effect of parameter value variations on the output delay is reduced. We model the variation shielding phenomenon for each parameter p by the following expression:

$$\sigma_p\,(segment_i) = \alpha \times \sigma_p\,(segment_{i-1}) \qquad (4.1)$$

where $\sigma_p\,(segment_i)$ is the variance of a parameter p of segment i. $1 \le i \le 10$ and $\alpha < 1$; α is set to 0.95 in our heuristic tool. Having selected the values for each segment, the model reduction is applied by using these modified values and the values of each circuit parameters in the reduced model specified.

We then repeat the experiments corresponding to Figure 4 using the values found through our heuristic. The results are shown in Figure 5. Compared to Figure 4, the pessimism is drastically reduced (e.g., for the case of 2RC-π model from 7.9% to 4% error in μ+3σ and from 3.2% to 1.4% error in mean, if α=0.95.) The intuitive reason is that the in case of the summation of the distributed parameters to a single value, the variations tends to cancel each other and thus the pessimism of the conventional approach for the extraction of a single component is reduced.

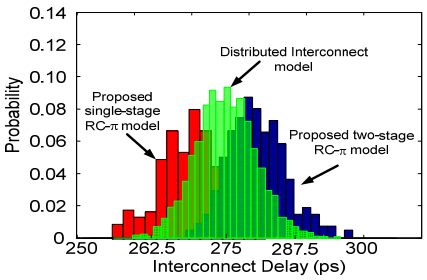


Figure 5: Accuracy improvement of 2RC- π crosstalk models.

4.3 Analytical Crosstalk-Aware Delay Analysis

The simulation setup of 3.2 is used to derive the mean and variance of crosstalk-aware output delay of the victim vs aggressor and victim line widths. They are shown in Figure 6 and Figure 7, respectively. Similar simulations have been performed considering different physical and electrical parameters. Each point in these figures is the result of 2500 sampled data in a Monte Carlo based environment. The large sampled data of 2500 points guarantees that the sample means have a normal distribution and that the closed form expression to model the effect of process variations on delay are accurate.

There is a tradeoff for the level of accuracy and complexity of closed-form expressions. As the number of input parameters increase, lower order models such as linear modeling of variation becomes more suitable. According to our experimental setup, we found the 2nd order modeling to be the most effective for the distribution properties of crosstalk-aware output delay and transition time of the victim line:

$$mean\ (delay\ ) = \sum_{parameter\ \ i} (A_i x_i^2 + B_i x_i) \quad (4.2)$$

$$\text{var}\ iance\ (delay\ ) = \sum_{parameter\ \ i} (C_i x_i^2 + D_i x_i) \quad (4.3)$$

$$mean\ (transition\ \ time\ ) = \sum_{parameter\ \ i} (E_i x_i^2 + F_i x_i) \quad (4.4)$$

$$mean\ (transition\ \ time\ ) = \sum_{parameter\ \ i} (G_i x_i^2 + H_i x_i) \quad (4.5)$$

where coefficients A_i to H_i are empirically found by using our statistical analysis and curve fitting of the results.

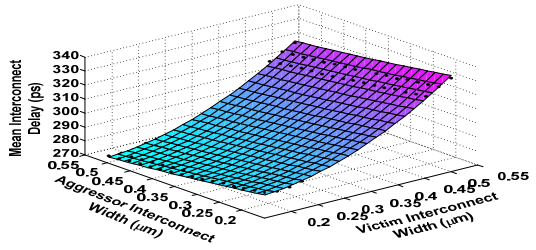


Figure 6: Crosstalk-aware victim interconnect delay (mean)

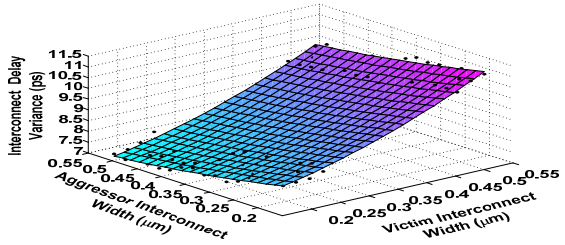


Figure 7: Crosstalk-aware victim delay (variance)

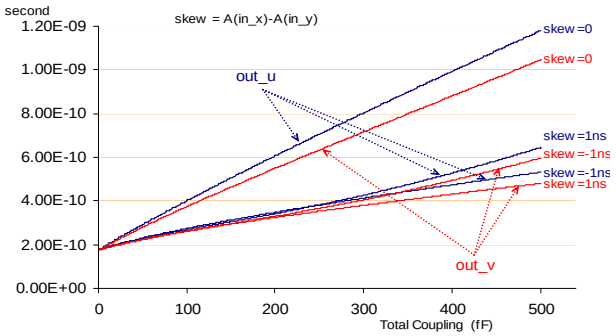
4.4.1. Sensitivity Analysis

To increase the efficiency of Equations (4.2) to (4.5.) we performed an extensive sensitivity analysis of crosstalk-affected delay to all circuit parameters to able to choose the right model (linear or higher order model) with respect to each parameter. The distributed circuit model of Figure 3 was used. Figure 8 illustrates an example of such experiments, which is the sensitivity of crosstalk-aware delay to the coupling capacitance value. The following observations were made with respect to each parameter:

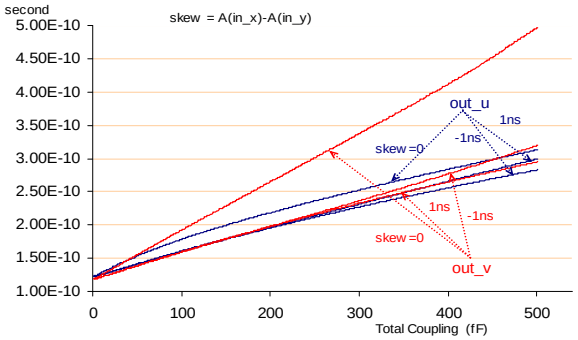
P1: Both crosstalk-affected output delay and transition time of the victim line are highly sensitive to the coupling capacitance value. Furthermore, both of these quantities are well approximated by assuming a linear dependence on the coupling value.

P2: Both crosstalk-affected output delay and transition time are moderately sensitive to the wire capacitance value. The delay monotonically increases as the victim wire capacitance increases; however, it does not show a monotone behavior with respect to the aggressor wire capacitance. Also, the output transition time does not exhibit a monotone relationship with respect to the wire capacitance of the victim or the aggressor line (cf. Figure 9.)

P3: The crosstalk-affected output delay and transition time are weakly sensitive to the wire resistance value. In particular, they monotonically increase as the victim wire resistance increases, while monotonically decreasing as the aggressor wire resistance increases. In both cases the effect can be well approximated by linear equations.



(a)



(b)

Figure 8: (a) Delay (from in_x (in_y) to) out_u (out_v) vs. coupling for three different input skew values. (b) Transition Time of out-u (out_v)

The above observations are helpful to decide whether a linear or a higher order model should be used with respect to each parameter in Equations (4.2) to (4.5). For example a linear modeling is enough for the case of resistance and coupling values, however for wire capacitance a 2nd or higher order model is necessary.

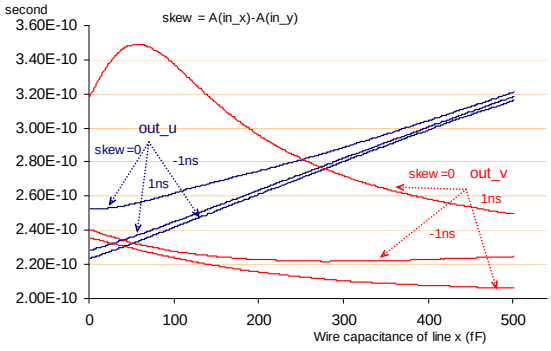


Figure 9: Transition times of out_u and out_v vs. wire capacitance of line x for different input skew values.

Figure 10 shows the fitted curve for the distribution of crosstalk-aware output delay of the victim line.

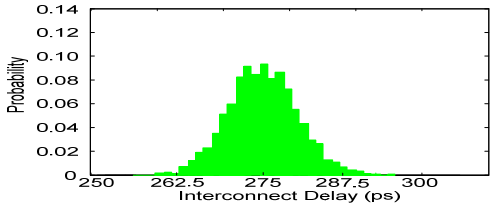
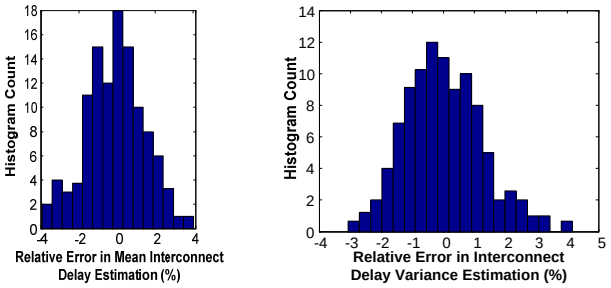


Figure 10: Crosstalk-aware output delay distribution for a 1mm long metal-4 interconnect pair

To evaluate the accuracy of our statistical expressions, we tested many cases of coupled interconnects from various sections of an industrial design by using Hspice. We then compared the results with those found by using our statistical expressions. Figure 11 illustrates the corresponding results. The average and maximum error magnitude for the mean calculation of crosstalk-aware delay are 1.7% and 5.1% respectively. The corresponding errors for variance are 1.3% and 3.9% respectively.



(a) (b)

Figure 11: Accuracy comparison vs. Hspice a) Mean Interconnect delay b) Interconnect delay variance

Performing Hspice-based study of the coupled interconnects while using the distributed RC-π model resolves the shortcomings of the previous approaches which rely on simpler, yet less accurate, circuit or waveform models. To increase the reliability of our statistical model, we had to simulate our circuit model under the whole range of physical parameters as well as variations in the input timing parameters, namely, skew and input transition times, for many coupled interconnects with different geometries. This kind of extensive simulation is required to be run only once per each process technology. The resulting statistical crosstalk-aware delay expressions can subsequently be used throughout the whole design and testing stages.

5. CONCLUSIONS

We proposed a statistical modeling to capture the effect of process variations on crosstalk-affected delay of coupled interconnects considering the large impact of correlation. A local process variation-aware distributed RC-π circuit modeling is developed for coupled interconnect pairs. Extensive Monte Carlo based Hspice simulations were to calculate the statistical properties of crosstalk with respect to variations in physical parameters and closed-form expressions for mean and variance have been derived. These expressions are shown to have near-to-Hspice accuracy. A statistical analysis method was also presented which is based on a heuristic that is applied prior to model order reduction so as to modify the values of the parameters such that process variations are properly accounted for. The effectiveness of this heuristic algorithm is confirmed for reduced models, namely, single and two RC-π crosstalk site models.

6. REFERENCES

[1] C. Visweswariah, "Death, taxes and failing chips" *Proc. of Design Automation Conf.* (*DAC*), pp. 343-347, 2003.

[2] M. Martina, G. Masera, "A statistical model for estimating the effect of process variations on crosstalk noise," *Proc. of the International Workshop on System level Interconnect Prediction* (*SLIP*), pp. 115-120, 2004.

[3] M. Agarwal, K. Agarwal, D. Sylvester, D. Blaauw, "Statistical modeling of cross-coupling effects in VLSI interconnects," *Proc. of Asia-Pacific Design Automation Conference*, (*ASP-DAC*), Vol. 1, pp. 503-506, 2005.

[4] T. Chen, A. Hajjar, "Statistical timing analysis of coupled interconnects using quadratic delay-change characteristics", *IEEE TCAD of Integrated Circuits and Systems, vol. 2312*, pp. 1677-1683, 2004

[5] S. Nazarian, M. Pedram, E. Tuncer, "An empirical study of crosstalk in VDSM technologies," *Proc. of Great Lake Symposium of VLSI*, (*GLSVLSI*), pp. 317-322, 2005

[6] A. Odabasioglu, M. Celik and L. Pileggi, "PRIMA: passive reducedorder interconnect macromodeling algorithm," *IEEE Trans. on CAD, vol. 17, No. 8*, pp. 645-653, 1998.

[7] P. Li, F. Liu, X. Li, T.L. Pileggi S.R. Nassif, "Modeling interconnect variability using efficient parametric model order reduction," *Proc. of Design, Automation, and Test in Europe*, (*DATE*), pp. 958-963, 2005.

[8] W.Y. Chen, S.K. Gupta, M.A. Breuer, "Analytial models for crosstalk excitation and propagation in VLSI circuits," *IEEE TCAD, Vol. 21 No. 10*, pp. 1117-1131, 2002.

[9] J. Cong, D. Pan, P.V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization," *Proc. of ASP-DAC*, pp. 373-378, 2001.

[10] M.R. Becer, D. Blaauw, V. Zolotov, R. Panda, I.N. Hajj, "Analysis of noise avoidance techniques in DSM interconnects using a complete crosstalk noise model," *Proc. of DATE*, pp. 456-463, 2002.

[11] P. Heydari, M. Pedram, "Analysis and reduction of capacitive coupling noise in high-speed VLSI circuits," IEEE *TCAD, vol. 24, Issue 3*, pp. 478-488, 2005.

[12] N. NS, T. Bonifield, A. Singh, C. Bittlestone, U. Narisimha, V. Le, A. Hill, " BEOL variability and impact on RC extraction," *Proc. of DAC*, pp. 758-759, 2005.

[13] B. Biswas "Modeling in-die process variation with accuracy," http://www.eetimes.com/story/OEG20040115S0027.

[14] S. Nassif, et al, "A methodology for modeling the effects of systematic with-in die variation," *Proc. of DAC*, pp. 172-175, 2000.

[15] J.H. Chern, J. Huang, L. Arledge, P.C. Li, P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," *Elc. Dev. Letters, Vol. 13, Issue 1*, pp. 32-34, 1992.

[16] J. Le, X. Li, L.T. Pileggi, "STAC: Statistical timing analysis with correlation," *Proc. of DAC*, pp. 343-348, 2004.

[17] A. Kahng, S. Muddu, D. Vidhani, "Noise and delay uncertainty studies for coupled RC interconnects," *Proc. of the International. ASIC/SOC Conference*, pp. 3-8, 1999.