A Life-Cycle Energy and Inventory Analysis of FinFET Integrated Circuits

Yanzhi Wang†, Ying Zhang‡, Mansour Rahimi‡, and Massoud Pedram†
†Department of Electrical Engineering
‡Department of Industrial and Systems Engineering
University of Southern California, Los Angeles, CA, USA
{yanzhiwa, zhan874, mrahimi, pedram}@usc.edu

***Abstract*—The manufacturing of modern semiconductor devices involves a complex set of nanoscale fabrication processes that are energy and resource intensive. There is a need for a comprehensive analysis of environmental impacts when an innovative new manufacturing approach emerges for semiconductor circuits. FinFET devices, a special kind of quasi-planer double gate devices, have been introduced as the next-generation semiconductor technology. This paper is the first attempt in reporting the life-cycle energy and inventory analysis of (double gate) FinFET integrated circuits. To make these results relevant, we have performed a comparative life-cycle analysis with the latest bulk CMOS technology. An inventory analysis is provided accounting for manufacturing, assembly, and use-phase. The functional unit used in this work is a processor with pre-specified levels of functionality and performance. Also, two types of applications are considered for this comparison: high-performance servers and low-power mobile devices. The results show that (i) FinFET circuits consume less use-phase energy compared with conventional CMOS counterparts, and (ii) FinFET circuits consume less manufacturing and assembly energy because the effect of smaller size outweighs that of more complex manufacturing process.**

***Index Terms*—FinFET; CMOS; life-cycle analysis; energy consumption; manufacturing**

I. INTRODUCTION

Semiconductor devices and circuits are ubiquitous components of modern electronics. Device fabrication involves a complex set of nanoscale fabrication processes, which are energy and resource intensive and generate significant waste. Life-Cycle Assessment (LCA) has been increasingly used to assess environmental implications of semiconductor device and circuit fabrication and usage [1]. An early study [2] highlighted the importance of assessing manufacturing and upstream environmental impacts associated with semiconductor devices. Murphy *et al.* presented a methodology for parametric semiconductor life-cycle inventory (LCI) models based on process specifications [3], whereas Yao *et al.* provided a comparative analysis of the manufacturing and consumer use phases of two generations of semiconductor devices [4]. Later work [5] provided a complete process-based life-cycle inventory for manufacturing of complementary metal oxide semiconductor (CMOS) logic circuits, which is the most common form of digital logic used in electronic circuits and systems today. This work was further extended in [6] by providing an LCA of CMOS logic chips over seven technology generations, spanning from 1995 to 2010. At a higher level than the semiconductor chips, reference works [7] and [8] studied the energy and material requirements associated with the manufacturing and use phases of information communication technology (ICT) products (i.e., personnel computers, mobile phones, embedded systems, etc.)

Technology advances of CMOS have followed Moore's law in the past 30 years, i.e., the number of transistors on integrated circuits doubles approximately every 18 months [9]. However, the conventional (bulk) CMOS technology cannot scale down beyond 16nm minimum feature size (also known as the technology node) because of the increasing leakage current and leakage power consumption induced by short-channel effects (SCEs) and the increasing variability levels induced by fundamental variations in a deeply scaled CMOS device, including random dopant fluctuation, line-edge roughness, and oxide thickness fluctuation [10].

To overcome the aforesaid drawbacks and thus enable the continuation of Moore's law to 7 or even 5nm technology nodes, (double gate) FinFET devices, a kind of special quasi-planar double gate device, have been developed and generally accepted as the next-generation device technology by major companies such as Intel, IBM, TSMC, and so on [11][12][13]. It is proved that FinFET devices and circuits can enhance the energy efficiency and soft-error immunity compared with their bulk CMOS counterparts. However, a comparative study of the life-cycle and environmental impacts of FinFET and conventional CMOS technologies is lacking. Although it is well-received that FinFET circuits incur lower use-phase energy consumption compared with CMOS and have smaller circuit area, the life-time energy consumption may actually be higher due to the more sophisticated manufacturing process [15] and the potentially lower yield.

In this paper, we present the first life-cycle energy and inventory analysis of FinFET devices and integrated circuits and a comparative analysis with bulk CMOS technology

devices and circuits. We provide an inventory analysis accounting for manufacturing, assembly, and use-phase. The functional unit used in this work is a (FinFET or bulk CMOS) processor with the same functionality and performance level. We first identify key differences between manufacturing FinFET and bulk CMOS devices, e.g., the spacer lithography process and the absence of channel doping and N-well/P-well manufacturing [15]. Next we generate the FinFET inventory in the manufacturing phase based on the conventional CMOS results [5]. We use the Poisson yield model [17] and perform sensitivity analysis on the defect rate of FinFET circuits/dies. For the use-phase electrical energy consumption, we consider two applications: high-performance servers and low-power mobile devices. We characterize energy consumptions of both FinFET and CMOS circuits in these two applications from accurate circuit simulations based on the 32nm Predictive Technology Models [18].

We briefly summarize the life-cycle energy consumption results as follows: (i) FinFET circuits achieve lower use-phase energy consumption compared with CMOS counterparts. (ii) When the fabrication defect rate of the FinFET circuit is the same as that of the conventional CMOS circuit, FinFET circuits consume less manufacturing and assembly energy because the effect of smaller circuit size outweighs that of more complex manufacturing process.

The rest of this paper is organized as follows: Section II provides an overview of the life-cycle assessment technique. Section III discussed our methods of life-cycle energy and inventory analysis of FinFET integrated circuits. Section IV presents experimental results, followed by conclusions in Section V.

II. Overview of Life-Cycle Assessment

LCA has existed in concept and practice since the 1960s. Particularly during the past several decades, the ICT community has recognized LCA as a useful tool to quantify the environmental impacts of various products and services. Essentially, practitioners identify a system's scope and boundaries, then construct an inventory of the various material and energy flows occurring during extraction of raw materials, manufacturing and assembly, transportation and installation, and operations, through end of life of the system. Practitioners use these aggregated flows to determine the overall environmental impact using standardized impact factors and established impact assessment methodologies.

An alternative to the process-based LCA is economic input-output (EIO) LCA, an expeditious approach that avoids somewhat arbitrary boundaries within the supply chain [19]. In the EIO LCA, macroscale input-output models, which track activity across various economic sectors, link to average environmental impacts within each sector to provide a sense of a product's (or a service's) typical environmental footprint based on its associated materials and energy resources usage across each sector. Hybrid approaches, which mesh the consistency and specificity of the process-based LCA approach with the practicality and ease of use of the EIO LCA approach are also common [7].

III. Methods

In this paper we provide an inventory and energy analysis accounting for manufacturing, assembly, and use-phase. Figure 1 illustrates the scope and boundaries of this analysis. We provide a comparative analysis of FinFET integrated circuits with their CMOS counterparts. Extraction of raw materials is not included in this work due to the high level of uncertainty associated with such accounting [1]. In the following, we discuss details of the life-cycle inventory and energy analysis in the following aspects: functional unit selection, manufacturing phase, yield analysis, assembly phase, and use-phase.

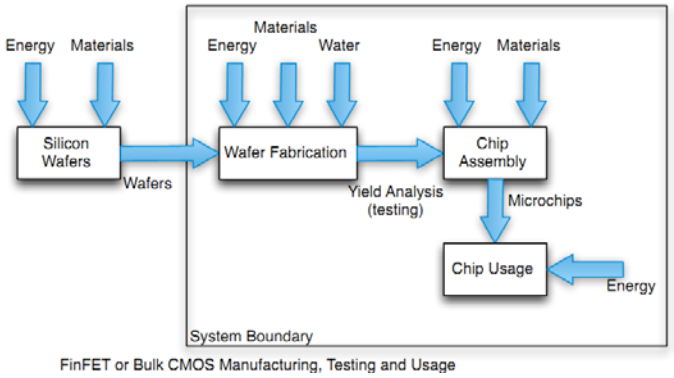

Figure 1. Product chain of (FinFET or bulk CMOS) semiconductor circuits, and system boundary of this work.

A. Functional Unit Selection

Choice of the functional unit drastically affects life-cycle impacts of semiconductor circuits, and there are arguments for every choice of functional unit, including, for example, an average device, a certain device area, a circuit comprising a given number of transistors or meeting some metric of computational power. Since the objective of this paper is to provide a comparative analysis of FinFET integrated circuits with bulk CMOS circuits, we set the functional unit to be a (FinFET or bulk CMOS) processor having the exact same functionality and performance level. We assume the same technology node, i.e., 32nm, for both FinFET and CMOS circuits for a fair comparison. Same functionality means that FinFET and bulk CMOS circuits have the same architecture and gate-level logic descriptions and in fact the same number of transistors with the same connections. Same performance level implies that FinFET and bulk CMOS circuits operate at the same frequency level, and thus, they can finish the same amount of computational tasks in a specified amount of time.

B. Manufacturing Phase

The main difference in the manufacturing of FinFET and bulk CMOS devices is twofold: (i) FinFET manufacturing requires additional steps to manufacture the "fin" structure. As illustrated in Figure 2, these fins can be formed by using

"spacers", formed along the sidewalls of a patterned sacrificial layer as a hard mask. An advantage of this spacer lithography process is that it provides for a doubling of the fin density, thereby reducing the circuit area. (ii) Unlike conventional CMOS devices, the channel (fin) of FinFET devices can remain undoped. The first difference requires additional steps in the FinFET manufacturing process whereas the second difference causes elimination of some steps in the conventional CMOS manufacturing process.

Reference [5] provides a complete process-based life-cycle inventory for manufacturing of conventional CMOS logic circuits. The whole process is divided into the silicon on insulator (SOI) module, the shallow trench isolation (STI) module, the gate module, and the interconnect module, with more than 100 detailed process steps. Detailed inventory for each step is provided in Table S3 to Table S17 in the supplementary materials of [5]. To reflect the difference between FinFET and conventional CMOS manufacturing processes in forming the fins, we add the following steps to the process flow of CMOS manufacturing (please refer to Figure 2 for the fin manufacturing process):

Wafer clean (0.035), Si deposit (7.6), Litho (2.8), Etch Si (1.5), PR Strip (1.2), Piranha clean (0.035), Deposit SiO_2 (7.1), Etch SiO_2 (2.6), Litho (2.8), Etch Si (1.5), Etch SiO_2 (2.6), PR Strip (1.2), Piranha clean (0.035)

We also show the energy consumption (in kWh) per 300 mm standard wafer for each new step. We also remove certain steps (related to channel doping) from the CMOS process flow because the channel (fin) of FinFET devices can remain undoped.

After we have determined the detailed process flow of FinFET manufacturing, we estimate the total manufacturing energy consumption per 300 mm standard wafer by summing up the energy consumption in each process step. As a result, the manufacturing energy per wafer is 421.74kWh for the bulk CMOS technology, and is 469.79kWh for the FinFET technology. This is because of the more sophisticated manufacturing process steps for the FinFET technology. In the same way, we calculate the material usage per wafer by summing up the material usage in each process step.

FinFET and bulk CMOS functional units may have different die areas, which also makes their energy consumptions different during the manufacturing phase. Reference [16] performed layout analysis and stated that, in general, FinFET standard cells can be more area-efficient than their bulk CMOS counterparts because of the vertical structure of fins and the spacer lithography technology. More specifically, FinFET standard cells can achieve area reduction ranging from nearly zero (for 1X INV, NAND, NOR, AOI gates) to more than 60% (for 8X INV, NAND, NOR, AOI gates) compared with their bulk CMOS counterparts, with an average area reduction of around 30%. We perform layout analysis on FinFET and bulk CMOS-based SRAM cells (used in register files and cache memory) and confirm 8% reduction in area when using FinFET technology compared with the bulk CMOS counterpart. We assume that for a conventional CMOS processor, 70% of the die area is utilized by logic cells and SRAMs, whereas 30% of the die area is taken by white space and VLSI interconnect, which is not scalable by using FinFET technology. Overall, we can achieve 12.5% overall area reduction in FinFET functional units when comparing with the CMOS counterparts.

We assume an area value of $1cm^2$ for the CMOS functional unit, which is the typical value for a CMOS processor [6]. For a standard 300 mm wafer using the CMOS technology, we can manufacture 654 gross dies (chips), but some of them may have defects and will be discarded in the subsequent testing procedure (only good dies will be packaged into integrated circuits)—we will analyze the yield in Section III.C. On the other hand, area of the FinFET functional unit is 0.875 cm^2. For a standard 300 mm wafer using the FinFET technology, we can manufacture 748 gross dies (chips) when neglecting yield.

In summary, we calculate the manufacturing energy per gross die using the following equation:

$$\frac{Manufacturing\ Energy\ per\ Wafer}{Number\ of\ Gross\ Dies\ in\ a\ Wafer} \quad (1)$$

The above calculation is used for both FinFET and conventional CMOS with different parameters. The overall material requirement can be calculated in the same way.

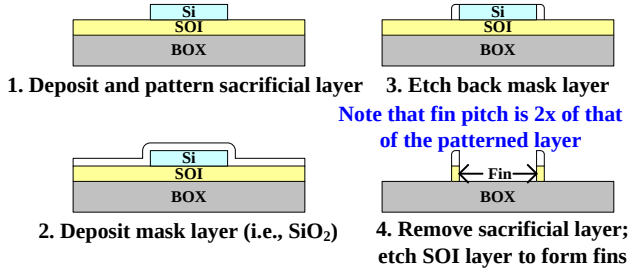

Figure 2. Sequence of schematic cross-sections illustrating the process for forming fins using sidewall spacers.

C. Yield Analysis

The yield is an important parameter in life-cycle assessment of semiconductor devices. A lower yield implies a higher expected manufacturing energy consumption per packaged functional unit. Because FinFET is an emerging technology compared with conventional CMOS and the yield data is not yet available, we perform a sensitivity analysis on the yield (or more specifically, the defect rate) of FinFET functional unit.

We adopt the Poisson yield model [17], which is a widely-used yield modeling technique in the semiconductor manufacturing and testing society. According to this model, the yield of a circuit with area A is given by $e^{-\lambda \cdot A}$, where λ is a parameter specifying the *defect rate* in circuit manufacturing. Since FinFET is a relatively new and emerging technology

compared with the matured CMOS technology, it is likely to have a relatively lower yield, i.e., a higher defect rate, λ.

We utilize the yield data in [5] for the state-of-the-art conventional CMOS functional unit, i.e., 88% line yield from wafer starts to finished wafer and 75% total yield from wafer starts to finished product [14]). Recall that the area values of FinFET and bulk CMOS functional units are 0.875cm^2 and 1cm^2, respectively. Hence, when the defect rate of FinFET technology is the same as bulk CMOS technology (i.e., when the FinFET technology is matured), the overall yield of the FinFET functional unit is 77.8%. This value is even higher than the yield of bulk CMOS functional unit because of the smaller area. On the other hand, when the defect rate of FinFET technology is 2X that of CMOS technology (i.e., when the FinFET technology is not yet matured), the overall yield of the FinFET functional unit is only 60.5%.

In summary, the overall (expected) manufacturing energy consumption of a functional unit is given by:

$$\frac{Manufacturing\ Energy\ per\ Gross\ Die}{Yield\ per\ Gross\ Die} \quad (2)$$

when the circuit yield is taken into account. The above calculation is used for both FinFET and bulk CMOS functional units with different parameters. The overall material requirement considering the circuit yield can be calculated in the same way.

D. Assembly Phase

Assembly is the encasing of rectangular segments of fabricated dies (circuits) into a protective package with external leads ("the black box with silver legs") [20]. We consider plastic packages which is by far the most commonly utilized. A lead frame, made of iron alloy with nickel or copper, forms the physical skeleton of the package and also provides the external leads in the final chip. We adopt the quantitative information from the MCC report [21], stating that the energy usage in the packaging stage is 0.34kWh per cm^2 of silicon. For the material usage, JEIDA publishes that 30g of packaging material per cm^2 of input silicon was consumed by the Japanese national industry [22]. Since the FinFET functional unit (processor) has a smaller area (0.875 cm^2) compared with the conventional CMOS one (1cm^2), the former will also result in less energy consumption in the assembly phase.

E. Use-Phase

We derive the use-phase electrical energy consumption of a functional unit for both FinFET and bulk CMOS technologies. We consider two applications: high-performance servers and low-power mobile devices. We use Intel Core2Duo E6850 as the example for the high-performance server application, with high performance, and 21.52W average power consumption during operation (averaged between its six voltage/frequency levels). We further assume that the server is used in a datacenter in a company such as Google, Amazon, etc., and is turned on 24 hours a day and has 33% activity factor (duty ratio) [8]. On the other hand, we use Samsung Exynos 4210 as the example of low-power mobile applications, with 1.2W average power consumption during operation time. We further assume that the mobile device (i.e., smartphone) is turned on 3 hours per day and has 15% activity factor (duty ratio) [8]. The life time of both applications is assumed to be 18 months.

Recall that we set the functional units to operate at the same frequency (and performance) level for both FinFET and conventional CMOS technology. For each type of application, we need to properly set the supply voltage V_{dd} levels such that the FinFET and conventional CMOS circuits operate at the same frequency level. We use the default V_{dd} level, i.e., 0.9 V, for the 32nm bulk CMOS technology, and derive the V_{dd} level that results in the same frequency for FinFET circuits based on simulations on benchmark circuits, including inverter chain, adders, and other digital circuit blocks. We use the 32nm Predictive Technology Models [18] for circuit simulations. In general, FinFET circuits require a lower V_{dd} level compared with CMOS circuits to operate at the same clock frequency because FinFET devices have stronger control over the channels (fins) and present less parasitic capacitances.

As long as the V_{dd} level of FinFET circuits is properly set, we can characterize the power consumptions, including both dynamic power and leakage power consumptions for both FinFET and bulk CMOS benchmark circuits. In general, FinFET circuits have lower power consumption because of the following reasons: (i) FinFET circuits have a lower V_{dd} level (around 0.8V), (ii) FinFET circuits have a lower dynamic power consumption due to the reduction of switching capacitances, and (iii) FinFET circuits also have a lower leakage power consumption because of the stronger control over the channels (fins).

After we have derived the power consumption results, we scale the power consumption of the FinFET functional unit based on the default values (21.52W for high performance applications and 1.2 W for low power applications) of the conventional CMOS functional unit. As one expects, the FinFET functional unit will incur lower use-phase energy consumption compared with the bulk CMOS one.

IV. Life-Cycle Energy Consumption Results

We summarize the life-cycle energy consumption results in these two applications in the following Table I, with two different defect rates of FinFET circuits/dies (the same and 2X of bulk CMOS defect rate). In this table, "HP" and "LP" denote "high performance" and "low power", respectively, whereas "LR" and "HR" mean "low defect rate" and "high defect rate", respectively, for the emerging FinFET technology. For the high performance server application with both higher power consumption and higher duty ratio, the use-phase energy consumption dominates the overall life-cycle energy consumption in both FinFET and bulk CMOS-based functional units (processors with the same functionality and performance level). On the other hand, for the low power mobile device with both lower power consumption and lower duty ratio, the

manufacture plus assembly energy consumption dominates the overall life-cycle energy consumption in both FinFET and bulk CMOS-based functional units. This conclusion is similar to that in [8].

When comparing between FinFET and bulk CMOS technologies, we can make the following three observations: (i) FinFET circuits achieve lower use-phase energy consumption compared with their bulk CMOS counterparts. This is because FinFET circuits have both lower leakage energy consumption and lower dynamic energy consumption due to the lower switching capacitance value. (ii) When the defect rate of FinFET circuit is the same as that of the bulk CMOS circuit, FinFET circuits achieve less manufacturing and assembly energy because the effect of smaller size of FinFET circuits outweighs that of more complex process. (iii) When the defect rate of FinFET circuit is twice that of the bulk CMOS circuit, FinFET circuits result in larger manufacturing energy because of the dominant impact of lower yield.

In summary, the adoption of FinFET technology will result in a reduction in life-cycle energy consumption in high performance applications even when the defect rate of FinFET circuits is high (FinFET technology is not matured yet). On the other hand, FinFET technology may in fact result in an increase in life-cycle energy consumption in low power applications when it has a higher defect rate than its bulk CMOS counterpart.

Table I. Life-cycle energy consumption results in high performance and low power applications of FinFET and CMOS functional units.

	Manufacture+ Assembly Energy	Use-Phase Energy	Total Energy
CMOS, HP*	1.32 kWh	93.4 kWh	94.7 kWh
FinFET, HP, LR	1.21 kWh	69.4 kWh	70.6 kWh
FinFET, HP, HR	1.48 kWh	69.4 kWh	70.9 kWh
CMOS, LP	1.32 kWh	0.296 kWh	1.62 kWh
FinFET, LP, LR	1.21 kWh	0.231 kWh	1.44 kWh
FinFET, LP, HR	1.48 kWh	0.231 kWh	1.71 kWh

*"HP", "LP" mean "high performance", "low power", respectively; "LR", "HR" mean "low defect rate", "high defect rate", respectively.

V. CONCLUSION

In this paper, we describe the first attempt at a comparative life-cycle energy and inventory analysis between the (double gate) FinFET integrated circuits and those of a conventional CMOS technology. We provide an energy and inventory analysis accounting for manufacturing, assembly, and use-phase. The functional unit used in this paper is a processor with equivalent levels of functionality and performance. We consider two applications: high-performance servers and low-power mobile devices. We have observed that (i) FinFET circuits consume less use-phase energy compared with bulk CMOS counterparts, and (ii) FinFET circuits consume less manufacturing and assembly energy, primarily due to its smaller size.

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