Balanced Reconfiguration of Storage Banks in a Hybrid Electrical Energy Storage System

Younghyun Kim[1], Sangyoung Park[1], Yanzhi Wang[2], Qing Xie[2],
Naehyuck Chang[1], Massimo Poncino[3], and Massoud Pedram[2]
[1]Seoul National University, Korea, [2]University of Southern California, CA, USA, [3]Politecnico di Torino, Italy
Email: [1]{yhkim, sypark, naehyuck}@elpl.snu.ac.kr, [2]{pedram, yanzhiwa, xqing}@usc.edu, [3]massimo.poncino@polito.it

***Abstract*—Compared with the conventional homogeneous electrical energy storage (EES) systems, hybrid electrical energy storage (HEES) systems provide high output power and energy density as well as high power conversion efficiency and low self-discharge at a low capital cost. Cycle efficiency of a HEES system (which is defined as the ratio of energy which is delivered by the HEES system to the load device to energy which is supplied by the power source to the HEES system) is one of the most important factors in determining the overall operational cost of the system. Therefore, EES banks within the HEES system should be prudently designed in order to maximize the overall cycle efficiency. However, the cycle efficiency is not only dependent on the EES element type, but also the dynamic conditions such as charge and discharge rates and energy efficiency of peripheral power circuitries. Also, due to the practical limitations of the power conversion circuitry, the specified capacity of the EES bank cannot be fully utilized, which in turn results in over-provisioning and thus additional capital expenditure for a HEES system with a specified level of service.**

This is the first paper that presents an EES bank reconfiguration architecture aiming at cycle efficiency and capacity utilization enhancement. We first provide a formal definition of balanced configurations and provide a general reconfigurable architecture for a HEES system, analyze key properties of the balanced reconfiguration, and propose a dynamic reconfiguration algorithm for optimal, online adaptation of the HEES system configuration to the characteristics of the power sources and the load devices as well as internal states of the EES banks. Experimental results demonstrate an overall cycle efficiency improvement of by up to 108% for a DC power demand profile, and pulse duty cycle improvement of by up to 127% for high-current pulsed power profile. We also present analysis results for capacity utilization improvement for a reconfigurable EES bank.

***Index Terms*—bank reconfiguration; hybrid electrical energy storage system**

I. Introduction

Electrical energy is a high-quality form of energy in the sense that it can be easily and efficiently converted into other forms of energy and furthermore it can be used to control other forms of energy [1]. Faced with a dramatic increase in demand for electrical energy for all kinds of socio-economic activities ranging from manufacturing, commerce, home entertainment, information technology equipment and devices, emerging (hybrid) electric vehicles, etc., economical use of electrical energy has become a first-priority issue of global importance. Electrical energy usage changes over time due to the types of load devices and user behaviors. Fossil fuel power plants and nuclear power plants can generate steady amount of power, but the amount of power generation is not immediately controllable. Furthermore, the output power levels of most renewable power sources are not controllable and are largely dependent on the environmental factors (e.g., the irradiance level or the climate condition.) Therefore, electricity supply (generation) and demand (consumption) are typically not balanced with each other. Storage of excessive energy and compensation of the energy shortage (or avoiding waste of energy) can significantly mitigate the under (or over)-investment in the generation facilities. Electrical energy storage (EES) systems can thus increase power reliability and efficiency, compensate the supply-demand mismatch, and regulate the peak-power demand.

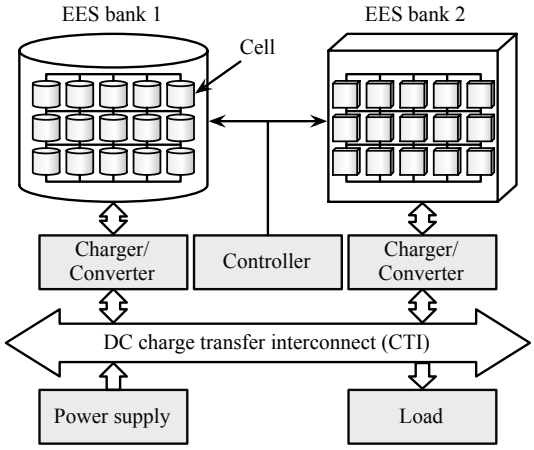

Fig. 1. Hybrid electrical energy storage (HEES) architecture.

A HEES (hybrid EES) system is an EES system that consists of two or more heterogeneous EES elements [2], [3]. No single EES element can fulfill all the requirements of electrical energy storage and retrieval operations, and it is not likely to have an ultimate high-efficiency, high power/energy capacity, low cost, and long cycle life EES element any time soon. Therefore, we use heterogeneous EES elements to hide drawbacks of each type while exposing their strengths. A simple structure of HEES systems is found in advanced electric vehicles, especially for efficient regenerative braking systems. A generalized HEES system architecture was recently introduced in [2].

A HEES system consists of heterogeneous EES banks, and each bank is composed of homogeneous EES elements cells as illustrated in Fig. 1. Energy is transferred between banks, from a bank to the load, or from the power supply to a bank over a DC charge transfer interconnect (CTI). Power converters are placed in between the CTI and EES banks for regulating voltage and/or current. A bank is typically organized as a two-dimensional array structure with a number of parallel and series connections of cells in order to provide more output power, larger energy capacity, or higher voltage level. The power capacity and voltage rating are determined by the number of parallel and series connections. When designing an EES bank structure, one should carefully determine the number of parallel and series connections of the cells since the organization directly impacts the energy efficiency. An improper bank structure design may result in significant cycle efficiency degradation during operation. However, it is hard to determine the optimal EES bank structure at design time because the characteristics of the power sources and load devices during operation of HEES systems as well as the internal state of the bank is not known at that time, and thus, a fixed array structure for the EES bank does not ensure consistent high efficiency at all times

subject to changes in the environmental and/or operating conditions of the bank. For instance, the conversion efficiency varies in a very wide range, and thus the power loss in the power converter is not negligible. Improper number (either too many or two few) of series connection of supercapacitor cells in a bank can result in serious imbalance between the CTI voltage and the bank voltage, which in turn results in a low efficiency for the power converter that sits between the bank and the CTI.

More importantly, the energy efficiency of the EES bank is heavily dependent on its internal state such as SoC (state of charge) and output terminal voltage. For example, supercapacitors are subject to a wide terminal voltage variation according to their SoC change due to the nature of capacitors. Even with elaborated careful initial determination of the number of series connections of supercapacitor cells, a severe imbalance between the CTI voltage and the bank voltage can develop anytime as a result of the change in the bank's SoC. Therefore, a fixed structure of an EES bank can hardly produce a steady high efficiency, and so run time reconfiguration is needed to dramatically enhance the overall HEES system efficiency.

In addition, practical power conversion circuits operate in a rather limited range of voltage and current levels. Due to the minimum voltage limitation, an EES bank cannot be fully discharged until the stored energy is completely retrieved. In other words, the capacity is not fully utilizable; instead, only a portion of the EES bank is effectively used to cycle (receive, store, and supply) energy.

This is the first paper that introduces a dynamic HEES bank reconfiguration method considering power conversion issues as the first step in order to realize higher cycle efficiency and storage capacity utilization with minimum HEES system cost. Previous research [4], [5], [6] has focused only on reconfiguration schemes considering the EES bank only, ignoring the power conversion issues. We expand the optimization scope to include the power converter, and minimize the energy loss in the converter, which is primarily caused by imbalance between the CTI voltage and the EES bank terminal voltage. Most of all, this paper introduces a general balanced bank reconfiguration for HEES systems. Objectives of the proposed reconfiguration method are: i) cycle efficiency improvement by voltage adaptation to increase power conversion efficiency, and ii) capacity utilization improvement by extracting as much energy as possible from an EES bank. The contributions of this paper are threefold; i) we introduce a formal definition of balanced reconfiguration of EES banks, ii) we propose a general balanced reconfiguration architecture for an EES bank and analyze the properties of the balanced configurations, and iii) we present a dynamic reconfiguration method for the proposed reconfigurable EES banks. Experimental results demonstrate dramatic energy efficiency and capacity utilization improvement achieved by supercapacitor bank reconfiguration.

II. Related Work

Some recent work introduce the concept of the HEES systems and explore the potential of the HEES systems making use of various energy storage devices [2], [3]. Among the various kinds of energy storage elements, supercapacitors are receiving more and more attention thanks to their superior cycle efficiency, long cycle life, and high volumetric power density. Such advantages make supercapacitors most suitable for frequently cycled power systems [7] and high power demand applications [8].

Dynamic reconfiguration of supercapacitor bank has been investigated by researchers for various purposes. Although there are a number of previous work that propose reconfiguration of an EES bank, there has been no attempt to explicitly take the power conversion efficiency into account from the holistic view of the HEES system. First of all, how to practically reconfigure the bank has been one concern of researchers. Power switches and diodes can compose paths to adaptively change the series-parallel connections of the supercapacitors [4], or selectable intermediate taps are used to progressively increase/decrease the number of charging or discharging supercapacitors [5], [9].

Batteries are another widely used EES elements these days. Large-scale battery bank management systems have been studied for fault tolerance [10]. A battery bank management scheme uses parallel, series, and bypass switches, to enhance battery life, flexibility, and to provide fault tolerance [11]. A multi-cell design which exploits battery characteristics such as recovery effect focuses on extending battery lifetime [12].

A recent work points out that very inefficient operation of supercapacitors takes place during startup (charging from empty SoC), and proposes to use a small supercapacitor during startup, and add up a larger reservoir supercapacitor later [13]. Some supercapacitors in a bank may fail and cause an open-circuit or a short-circuit fault, and then a dynamic reconfiguration may help increase the availability of the bank with degraded performance by excluding the failed cells [14]. A recent publication analyzes a switch-based shift circuit of a supercapacitor bank for rough voltage regulation as well as energy utilization improvement [6]. The rough voltage regulation, i.e., restricting the bank voltage variation, of [4], [5], [6] may help improve the power conversion efficiency, but provide no explicit clue which configuration should be used and when. This is because the previous dynamic reconfiguration research focused on the EES bank only, without consideration on the associated power delivery subsystems. Different from the previous work, we explicitly consider the power delivery subsystems into account when performing reconfiguration in order to find the true maximum-efficiency configurations.

III. HEES Systems

A. Power Converter Model

A power converter is to deliver regulated voltage or current at a desired level regardless of variation in the input power source and/or the load device. The power converter is an essential component to buffer the voltage or current mismatch between the CTI and EES bank, and to provide controlled power delivery. In this paper, each EES bank has two power converters, one for charging the EES bank, and the other for discharging the EES bank, as shown in Fig. 2. Generally speaking, the charging converter provides a regulated current output for the EES bank, and the discharging converter provides a regulated voltage output for the CTI. We assume both power converters are identical uni-directional switching buck-boost converters with the model shown in Fig. 2, but their directions are the opposite; the CTI is input and the EES bank is output for the charging converter, and the EES bank is input and the CTI is output for the discharging converter. Throughout this paper, the condition such that $I_{cti} > 0$ and/or $I_{bank} > 0$ implies a charging process, and the opposite condition such that $I_{cti} < 0$ and/or $I_{bank} < 0$ implies a discharging process.

Depending on the relation between V_{in} and V_{out}, a power converter has two working modes: buck (step-down) mode and boost (step-up) mode. As the names imply, power converters operate in the buck mode if $V_{in} > V_{out}$, and otherwise in the boost mode. An ideal power converter delivers the entire power from the source to the load without any loss, but the power conversion involves non-zero amount of power loss in practice. The power conversion efficiency η_{conv} is defined as

$$\eta_{conv} = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{conv}}{P_{in}} = \frac{V_{in} \cdot I_{in} - P_{conv}}{V_{in} \cdot I_{in}}, \qquad (1)$$

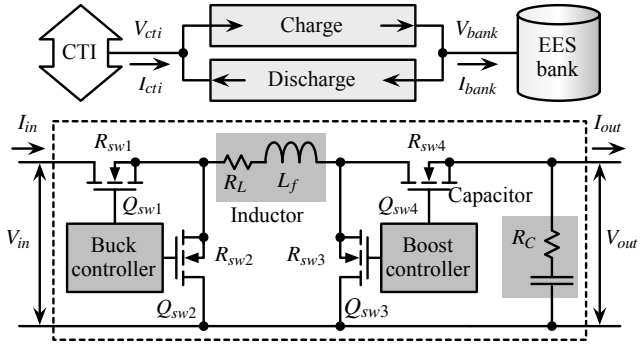

Fig. 2. Switching power converter for charging and discharging an EES bank.

where P_{in} and P_{out} is input and output power of the converter, respectively, and P_{conv} is the power loss during the power conversion. A common type of power converters that deals with medium to larger power capacity is a PWM (pulse width modulation) switching power converter. The power loss of the PWM switching power converter consists of three components: conduction loss P_{cdct}, switching loss P_{sw} and controller loss P_{ctrl} [15]. That is,

$$P_{conv} = P_{cdct} + P_{sw} + P_{ctrl}. \tag{2}$$

Those power loss components are strongly dependent on the input voltage V_{in}, output voltage V_{out}, output current I_{out}, and the circuit component properties.

In the buck mode, the power loss components can be expressed as

$$\begin{aligned} P_{cdct} =& {I_{out}}^2 \cdot (R_L + D \cdot R_{sw1} + (1-D) \cdot R_{sw2} + R_{sw4}) \\ &+ \frac{(\Delta I)^2}{12} \cdot (R_L + D \cdot R_{sw1} + (1-D) \cdot R_{sw2} + R_{sw4} + R_C), \\ P_{sw} =& V_{in} \cdot f_s \cdot (Q_{sw1} + Q_{sw2}), \\ P_{ctrl} =& V_{in} \cdot I_{ctrl}, \end{aligned} \tag{3}$$

where $D = \dfrac{V_{out}}{V_{in}}$ is the PWM duty ratio and $\Delta I = \dfrac{V_{out} \cdot (1-D)}{L_f \cdot f_s}$ is the maximum current ripple; f_s is the switching frequency; I_{ctrl} is the current flowing into the controller; R_L and R_C are the equivalent series resistance (ESR) of inductor L and capacitor C, respectively; $R_{sw1,\ldots,4}$ and $Q_{sw1,\ldots,4}$ are the turn-on resistances and gate charges of the four switches in Fig. 2, respectively.

In the boost mode, the power loss components can be expressed as

$$\begin{aligned} P_{cdct} =& \left(\frac{I_{out}}{D}\right)^2 \\ &\cdot (R_L + (1-D) \cdot R_{sw3} + D \cdot R_{sw4} + R_{sw1} + D \cdot (1-D) \cdot R_C) \\ &+ \frac{(\Delta I)^2}{12} \cdot (R_L + (1-D) \cdot R_{sw3} + D \cdot R_{sw4} + R_{sw1} + D \cdot R_C), \\ P_{sw} =& V_{out} \cdot f_s \cdot (Q_{sw3} + Q_{sw4}), \\ P_{ctrl} =& V_{in} \cdot I_{ctrl}, \end{aligned} \tag{4}$$

where $D = \dfrac{V_{in}}{V_{out}}$ and $\Delta I = \dfrac{V_{in} \cdot (1-D)}{L_f \cdot f_s}$.

B. Supercapacitor Model

Supercapacitors have very small internal resistance so that very small IR power loss is accompanied by the charging and discharging operations. Moreover, the supercapacitors exhibit a significant higher volumetric power density [16] and a longer cycle life [17] compared with batteries. These factors make supercapacitors attractive in dealing with frequent charging and discharging or intermittent high current pulsed charging and discharging.

Primary disadvantages of supercapacitors are a wide range of terminal voltage variation and a large self-discharge rate compared with other EES elements. A supercapacitor is inherently a capacitor whose terminal voltage V is linearly proportional to the amount of charge stored in the capacitor Q. Since the energy stored in a capacitor is $E = \dfrac{1}{2} \cdot C \cdot V^2$, its voltage is $V = \dfrac{Q}{C} = \sqrt{\dfrac{2 \cdot E}{C}}$, where C is its capacitance. Since E increases or decreases dynamically through charging or discharging operations, the voltage variation will be much higher than that of other EES elements. For example, the voltage is nearly 0 V when the supercapacitor is almost depleted, while a battery maintains marginally a constant voltage throughout the charge and discharge cycle. This shortcoming is the one of the major motivations of this work in that the varying voltage incurs a significant power conversion efficiency variation as described in Section III-A.

In addition, a supercapacitor may lose more than 10% of its stored energy per day even if no load is connected to it [2]. The voltage decay after a time period Δt is given by

$$V(t + \Delta t) = V(t) \cdot e^{-\Delta t / \tau}, \tag{5}$$

where τ is the self-discharge time constant.

Although the proposed EES bank reconfiguration architecture is generally applicable to any kinds of EES elements including batteries, we focus on the supercapacitor bank in this paper because the benefit of the reconfiguration is distinct for supercapacitors.

C. EES Banks Performance Metrics

Cost factors of HEES systems fall into two categories: operational cost and capital cost [2]. The operational cost is mainly the electricity cost, and thus it is directly related to the efficient use of energy. The capital cost includes expenses for purchasing and disposal of the EES elements, and therefore fully utilizing the EES bank capacity is a key for reducing the capital cost. Cycle efficiency and capacity utilization of EES banks are the major factors that motivate dynamic reconfiguration of EES banks for reducing the operational cost and capital cost of HEES systems.

The cycle efficiency is 'round-trip' energy efficiency generally defined as $\eta_{cyc} = \dfrac{E_{out}}{E_{in}}$ where E_{in} and E_{out} denote energy input and energy output, respectively. The cycle efficiency of supercapacitors is close to 100%, which means that almost all the energy consumed to charge a supercapacitor can be retrieved in the following discharging process. On the other hand, the cycle efficiency of batteries ranges 60–90% depending on the chemistry used for the electrodes even under the optimal charge and discharge condition.

The cycle efficiency generally has been considered as a natural characteristics of an EES element [17]. However, the cycle efficiency is closely related to the charge and discharge rates, i.e., the magnitude of charge and discharge current with respect to the rated capacity of the storage element. The rate capacity effect of batteries results a low cycle efficiency for a high-current charge and discharge. In practice, from the system-level point of view, one should not disregard the power conversion process and its power loss when considering the cycle efficiency of an EES bank. In fact, the cycle efficiency is significantly affected by the power conversion efficiency, which is also a function of the charge and discharge rates as discussed in Section III-A.

Therefore, it is beneficial to define constant-power charging efficiency η_c and constant-power discharging efficiency η_d for the cases

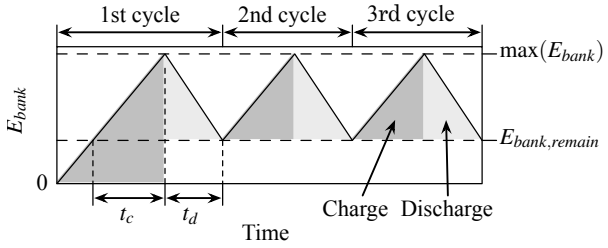

Fig. 3. Cycle efficiency and capacity utilization in repeated charge-discharge cycles.

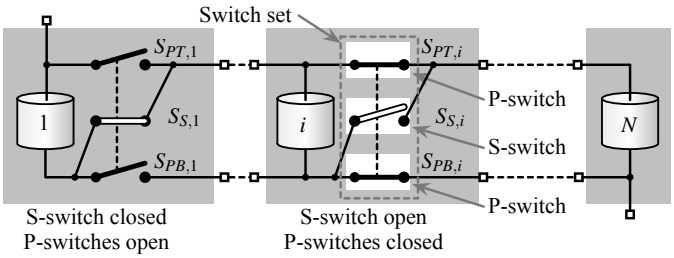

Fig. 4. General balanced reconfiguration architecture (GBRA) of an N-cell EES bank.

that a storage element is charged and discharged at a constant CTI power and a constant CTI voltage:

$$\eta_c(P_{cti,c},V_{cti}) = \frac{\max(E_{bank})}{P_{cti,c}\cdot t_c(P_{cti,c},V_{cti})}, \tag{6}$$

$$\eta_d(P_{cti,d},V_{cti}) = \frac{P_{cti,d}\cdot t_d(P_{cti,d},V_{cti})}{\max(E_{bank})}, \tag{7}$$

where $t_c(P_{cti,c},V_{cti})$ is the charging time, $t_d(P_{cti,d},V_{cti})$ is the discharging time, $P_{cti,c}$ is the CTI power when charging, $P_{cti,d}$ is the CTI power when discharging, and V_{cti} is the CTI voltage. As a result, the *constant-power cycle efficiency* η_{cyc} when $P_{cti,c} = P_{cti,d} = P_{cti,cyc}$ is defined as

$$\eta_{cyc}(P_{cti,cyc},V_{cti}) = \eta_c(P_{cti,cyc},V_{cti})\cdot\eta_d(P_{cti,cyc},V_{cti}). \tag{8}$$

In this paper, we define *capacity utilization* as one of the important performance metrics of an EES bank. A bank voltage cannot be arbitrarily low because the power converter cannot operate below a certain voltage [6], which we define as $V_{bank,min}$. The capacity utilization ρ is defined as the ratio between the usable energy capacity and the original energy capacity of the EES bank. The capacity utilization is equivalent to the ratio between the extracted energy and the stored energy in a fully charged bank. That is,

$$\rho = 1 - \frac{E_{bank,remain}}{E_{bank,lim}}, \tag{9}$$

where

$$E_{bank,remain} = \frac{1}{2}\cdot C_{bank}\cdot {V_{bank,min}}^2 \tag{10}$$

is the remaining energy when the power converter can no longer extract energy, i.e., loss in the capacity. The capacity utilization of storage elements is smaller than 100% because the power converter requires the minimum bank voltage, $V_{bank,min}$, which is higher than 0 V.

Fig. 3 illustrates the effect of the cycle efficiency and capacity utilization. The operational cost of HEES systems is affected mainly by the cycle efficiency. If the cycle efficiency is poor, we have to expense more for storing and retrieving the same amount of energy. As shown in Fig. 3, the very first cycle requires additional energy of $E_{bank,remain}$ to increase the bank voltage from 0 V to $V_{bank,min}$. The operational cost for this additional energy is dependent on the capacity utilization, but this effect may be neglected for repeated cycles in long term. The capital cost is affected by the effective energy capacity of the EES banks. If the capacity utilization is 80%, we lose 20% of the expenses for the storage elements because this portion does not contribute to the energy capacity.

IV. General Balanced Reconfiguration Architecture

In this paper, we introduce the *general balanced reconfiguration architecture* (GBRA) for the EES bank reconfiguration. We define a balanced reconfiguration to satisfy the condition whereby all energy storage cells in a given EES bank have identical SoC and terminal voltages at all times i.e., they are balanced at all times, given that the cells are healthy and identical. Unless active charge balancing circuits are used (which is not the case here), cell balancing can be achieved by regular arrangement of cells. We call such arrangements balanced configurations. The proposed architecture is 'general' in the sense that it can produce every balanced configuration that is possible with a given number of cells.

Let N denote the number of available cells. The N cells can be organized in various balanced configurations and the number of possible configurations equals the number of bi-factor decompositions of the natural number N (including $1\times N$ and $N\times 1$.) We define a configuration $\mathcal{C}(m,n)$ to be a configuration that has m cells in series and n cells in parallel. For example, the number of balanced configurations of a 10-cell bank (N is 10) is four: $\mathcal{C}(1,10)$, $\mathcal{C}(2,5)$, $\mathcal{C}(5,2)$, and $\mathcal{C}(10,1)$. Although $\mathcal{C}(3,3)$, which is composed of nine cells, is also possible with 10 cells, we do not consider such a case as a balanced configuration because it leaves one cell imbalanced.

Fig. 4 shows the proposed GBRA of a bank composed of N cells. Each of $N-1$ cells has three switches: one series switch (S-switch) and two parallel switches (P-switches) except for the last one. The P-switches connect cells in parallel into n-parallel sub-banks, whereas the S-switches connect those m sub-banks in series. A sub-bank is a set of cells connected only in parallel. For the i-th cell, its S-switch is denoted by $S_{S,i}$, while its two P-switches are denoted by $S_{PT,i}$ and $S_{PB,i}$, one on the top and the other in the bottom, respectively. We group the three switches of one cell as a switch set, which gives rise $N-1$ switch sets in the bank. For each cell, $S_{PT,i}$ and $S_{PB,i}$ are closed exactly if $S_{S,i}$ is open. There are no cases where one of $S_{PT,i}$ and $S_{PB,i}$ switches is open while the other is closed.

More formally, for $i = 1,2,\ldots,N-1$,

$$x_{P,i} + x_{S,i} = 1, \tag{11}$$

where

$$x_{S,i} = \begin{cases} 0 & \text{if } S_{S,i} \text{ is open,} \\ 1 & \text{if } S_{S,i} \text{ is closed,} \end{cases} \tag{12}$$

$$x_{P,i} = \begin{cases} 0 & \text{if } S_{PT,i} \text{ and } S_{PB,i} \text{ are open,} \\ 1 & \text{if } S_{PT,i} \text{ and } S_{PB,i} \text{ are closed.} \end{cases} \tag{13}$$

Otherwise, the bank malfunctions; more precisely, the i-th cell is disconnected from the $(i+1)$-th cell if $x_{S,i} = x_{P,i} = 0$, or the i-th supercapacitor is short-circuited if $x_{S,i} = x_{P,1} = 1$.

A balanced configuration of GBRA is obtained by switching operations which obeys the following rule; in the m-by$-n$ balanced

configuration $\mathcal{C}(m,n)$,

$$x_{S,i} = \begin{cases} 1 & \text{if } i = n \cdot k \text{ where } k = 1,2,\ldots,m-1, \\ 0 & \text{otherwise,} \end{cases} \tag{14}$$

$$x_{P,i} = 1 - x_{S,i}. \tag{15}$$

The total capacitance C_{bank}, voltage V_{bank}, internal resistance R_{bank}, and energy storage capacity E_{bank} of a bank of $\mathcal{C}(m,n)$ are calculated as follows:

$$C_{bank} = \frac{n}{m} \cdot C_{cell} = \frac{N}{m^2} \cdot C_{cell}, \tag{16}$$

$$V_{bank} = m \cdot V_{cell}, \tag{17}$$

$$E_{bank} = \frac{1}{2} \cdot C_{bank} \cdot {V_{bank}}^2 = N \cdot E_{cell}, \tag{18}$$

$$R_{bank} = \left(\frac{2}{3} \cdot n - 1 + \frac{1}{3 \cdot n} \right) \cdot m \cdot R_p + \frac{m}{n} \cdot R_c + (m-1) \cdot R_s, \tag{19}$$

where C_{cell}, V_{cell}, and E_{cell} denote the capacitance, voltage, and energy capacity of each cell, respectively; R_s and R_p denote the on-resistance of an S-switch and a P-switch, respectively; and R_c denotes the ESR of each cell. We assume that the charge or discharge current is equally distributed to every cell in a sub-bank when we derive (19). For a fixed N, the bank total capacitance C_{bank} is inversely proportional to m^2 whereas the bank terminal voltage V_{bank} is proportional to m. The total energy remains the same regardless of the configuration.

Each cell has its voltage limit $V_{cell,lim}$ that should not be exceeded, and corresponding energy capacity limit $E_{cell,lim}$. The voltage limit $V_{bank,lim}$ and energy capacity limit $E_{bank,lim}$ of a bank are defined similar to (17) and (18):

$$V_{bank,lim} = m \cdot V_{cell,lim}, \tag{20}$$

$$E_{bank,lim} = N \cdot E_{cell,lim}. \tag{21}$$

Fig. 5 is an example of reconfiguration of a four-cell bank ($N = 4$) with the GBRA. With four cells, three balanced configurations are possible. One of them, for example, is $\mathcal{C}(2,2)$ which consists of two sub-banks connected in parallel with P-switches, and each sub-bank composed of two cells connected in series with S-switches.

Fig. 6 shows the switch operations for each configuration when $N = 60$. Each row represents the configuration $\mathcal{C}(m,n)$, and each square represents which of the S-switch and P-switches are closed in the configuration. One can notice from the figure that each switch set has a different probability for closing the S-switch or P-switches. For example, $S_{S,30}$ is more likely to be closed than other S-switches in many configurations. On the other hand, switch sets that are annotated with dotted boxes always close P-switches except only for one configuration $\mathcal{C}(60,1)$. In general, $x_{S,i} = 1$ in $\mathcal{C}(m,n)$ exactly if n is a common divisor of i and N, otherwise, $x_{P,i} = 1$ as shown in (14).

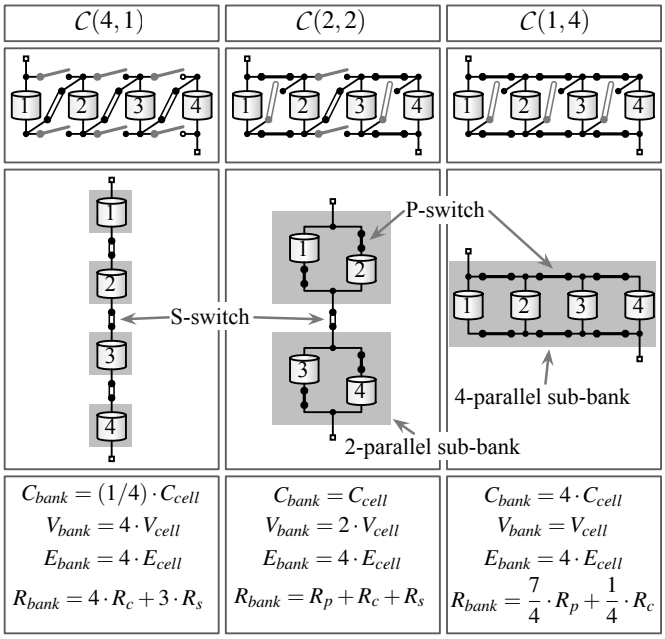

Fig. 5. Reconfiguration examples of a four-cell EES bank ($N = 4$).

This observation provides the intuition for an optimization method to reduce the number of switches. A switch set can be removed if the switches in the set do not change their states, i.e., they remain always open or always closed. An always-open switch may be removed from the circuit, while an always-closed switch may be replaced by a wire. Eliminating unnecessary switch sets not only reduces the overall switch implementation cost, but also reduces the bank internal resistance and in turn, lowers the IR loss.

We can reduce the number of switches by restricting possible configurations. More precisely, $S_{S,i}$ may be short-circuited, and $S_{PT,i}$ and $S_{PB,i}$ may be open if we use only configurations where n and i are coprime. Conversely, $S_{S,i}$ may be open, and $S_{PT,i}$ and $S_{PB,i}$ may be short-circuited if we never use configurations where n and i are coprime. In the previous example, out of the 59 switch sets, 16 switch sets that are annotated with the dotted boxes can be removed if $\mathcal{C}(60,1)$ is not used. However, we do not consider configuration selection as part of this paper, and assume all the configurations are possible with all the switch sets present.

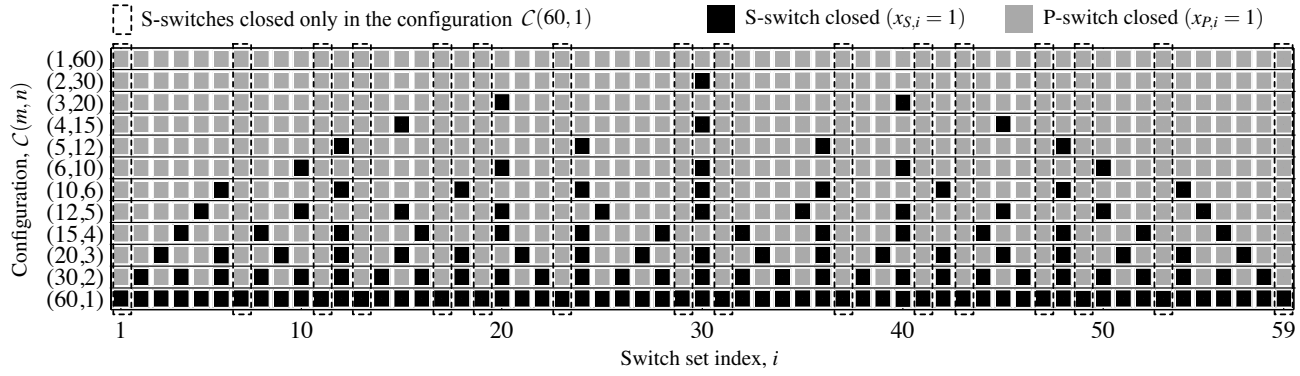

Fig. 6. Operations of S-switches and P-switches of a 60-cell bank in different configurations.

V. Dynamic EES Bank Reconfiguration Algorithm

A. Cycle Efficiency

The primary objective of the dynamic EES bank reconfiguration is reducing energy loss by improving the power conversion efficiency. As discussed in Section III-A, the power conversion efficiency of power converters depends on the input and output voltage and current values, that is V_{bank}, V_{cti}, I_{bank}, and I_{cti}. The purpose of dynamic EES bank reconfiguration is to maximize conversion efficiency η_{conv} by controlling V_{bank} at run time for given V_{cti} and I_{cti}. Meanwhile, the bank voltage should be within a range of $[V_{bank,min}, V_{bank,max}]$ as the power converter requires.

- **Given:** Number of cells N, CTI voltage V_{cti}, CTI current I_{cti}, and cell voltage V_{cell}.
- **Find:** Configuration $\mathcal{C}(m,n)$ that minimizes the power loss of the EES bank.
- **Subject to:** Bank voltage limitation: $V_{bank,min} \leq V_{bank} \leq V_{bank,max}$.

The power loss of the EES bank has two components: power conversion loss which is discussed in Section III-A, and IR loss induced by the internal resistance of the EES bank. Minimizing the power converter loss has different implications for charging and discharging: i) for charging, it means maximizing energy transferred from the CTI to the bank, and ii) for discharging, it means maximizing energy transferred from the bank to the CTI.

The dynamic reconfiguration is expressed as a mapping function

$$f : (V_{cti}, I_{cti}, V_{cell}) \rightarrow \mathcal{C}(m,n), \tag{22}$$

where $V_{cti,min} \leq V_{cti} \leq V_{cti,max}$, $I_{cti,min} \leq I_{cti} \leq I_{cti,max}$, $0 \leq V_{cell} \leq V_{cell,lim}$, $m \in M$, and $n = N/m$. Here, $[V_{cti,min}, V_{cti,max}]$ and $[I_{cti,min}, I_{cti,max}]$ denote the operational range of V_{cti} and I_{cti}, respectively, and M is a list of possible values of m in an ascending order. We can see that exhaustive online search for the optimal m and n among numerous configurations is not practical. Therefore, we propose a two-phase reconfiguration method, which consists of an offline phase and an online phase. In the offline phase, we analyze the power converter efficiency η_{conv} and develop a function $f_{offline}$ to find the optimal bank voltage $V_{bank,opt}$ for given V_{cti} and I_{cti}. Next, in the online phase, we use a function f_{online} to find the optimal configuration $\mathcal{C}(m,n)$ that minimized the power loss for given V_{cell}. That is,

$$f_{offline} : (V_{cti}, I_{cti}) \rightarrow V_{bank,opt}, \tag{23}$$

$$f_{online} : (V_{cti}, I_{cti}, V_{bank,opt}, V_{cell}) \rightarrow \mathcal{C}(m,n). \tag{24}$$

We cannot analytically find the optimal operating conditions that maximizes the power conversion efficiency η_{conv}. Therefore, it is reasonable to implement the offline function $f_{offline}$ as a lookup table since it is only two-dimensional and both of V_{cti} and I_{cti} have a limited range in practice because of the minimum and maximum ratings of peripheral circuitry. We build the lookup table by evaluating the conversion efficiency as described in Section III-A and finding the optimal condition. The lookup table is indexed with V_{cti} and I_{cti}, where each entry is the optimal bank voltage $V_{bank,opt}$ that maximizes η_{conv} for given V_{cti} and I_{cti}. Two lookup tables are built for charging and discharging in the same manner. The online algorithm can exploit these lookup tables and easily obtain $V_{bank,opt}$ at run time which greatly reduces the computation overhead.

The online function f_{online} is described in Algorithm 1. First, the optimal bank voltage is derived from $f_{offline}$ mapping function for current V_{cti} and I_{cti} (List 1). Since the lookup table is defined for discrete intervals, a two-dimensional interpolation may be used for intermediate values. Next, the ideal series-connection number m_{ideal} is derived (List 2). We redefine a possible set of configurations M' for the given condition, by excluding configurations that are not allowed due to bank voltage limitation (List 3). If m_{ideal} implies a possible configuration (List 4), this is the optimal value for m. However, it is possible that m_{ideal} represents not a feasible configuration. If m_{ideal} is out of boundary of possible configurations, we set m_{opt} to the minimum or maximum (Lists 6 and 8). Otherwise, we find a consecutive m_i and m_{i+1} in M' that are near m_{ideal} (List 11). Between two configurations, we select the one whose sum of the power converter loss and IR loss due to the bank internal resistance is smaller (List 12). Finally, n_{opt} is derived (List 13), and the optimal configuration is returned. This algorithm has $O(\log|M|)$ time complexity if M is in an ascending order, because finding elements in Lists 3 and 11 can be done with a binary search. Other operations are done in constant time; the lookup table indexing and the interpolating are done in constant time, and efficiency evaluation in List 12 is done only for two configurations regardless of the size of M.

Algorithm 1: f_{online}: Online optimal configuration determination.

Input: V_{cti}: CTI voltage, I_{cti}: CTI current, and V_{cell}: cell voltage
Output: Optimal configuration (m_{opt}, n_{opt})
Global: N: number of cells, M: list of possible values of m in an ascending order, $f_{offline}$: optimal bank voltage mapping function, P_{conv}: power converter loss model, P_{int}: bank internal resistance IR loss model, $[V_{bank,min}, V_{bank,max}]$: range of V_{bank}

1 $V_{bank,opt} = f_{offline}(V_{cti}, I_{cti})$
2 $m_{ideal} = \dfrac{V_{bank,opt}}{V_{cell}}$
3 $M' = \left\{ m \in M \middle| V_{bank,min} \leq m \cdot V_{cell} \leq V_{bank,max} \right\}$
4 **if** $m_{ideal} \in M'$ **then**
5 $m_{opt} = m_{ideal}$
6 **else if** $m_{ideal} \leq \min(M')$ **then**
7 $m_{opt} = \min(M')$
8 **else if** $m_{ideal} \geq \max(M')$ **then**
9 $m_{opt} = \max(M')$
10 **else**
11 Find i such that $m_i \leq m_{ideal} \leq m_{i+1}$, where $m_i, m_{i+1} \in M'$
12 $m_{opt} = \arg\min_{m} \left(P_{conv}(V_{cti}, I_{cti}, m \cdot V_{cell}) + P_{int}(m, I_{bank}) \right)$ for $m \in \{m_i, m_{i+1}\}$
13 $n_{opt} = \dfrac{N}{m_{opt}}$
14 **return** (m_{opt}, n_{opt})

In a discrete-time reconfiguration scheme, bank reconfiguration is performed every decision epoch, assuming that the voltage and current condition is not significantly changed within a time interval. On the other hand, in a continuous-time reconfiguration scheme, we determine whether if a reconfiguration is needed when the voltage or current condition significantly changes.

Fig. 7 shows two configuration transitions of a 120-cell bank when discharging. The figure shows transitions from $\mathcal{C}(24,5)$ to $\mathcal{C}(30,4)$, and from $\mathcal{C}(30,4)$ to $\mathcal{C}(40,3)$. The transitions occur at the points where the power loss (sum of power converter loss and internal resistance IR loss) of two consecutive configurations cross. This is different from a previous work [6] that the configuration transitions is triggered by the bank voltage variation constraint. Although limiting the bank voltage variation may improve the power

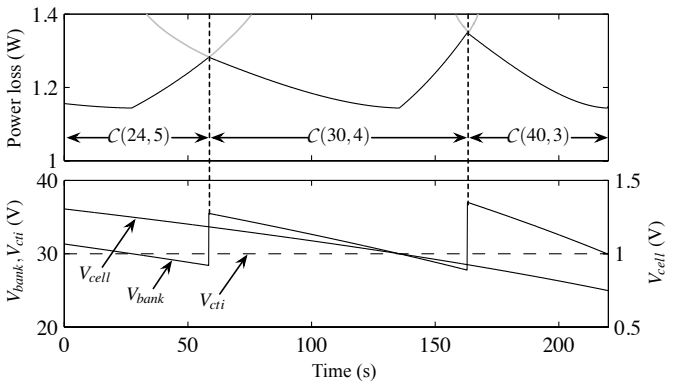

Fig. 7. Two configuration transitions before and after the configuration $\mathcal{C}(30,4)$ when discharging a 120-cell bank. CTI voltage (V_{cti}) is 30 V and CTI current (I_{cti}) is -1 A.

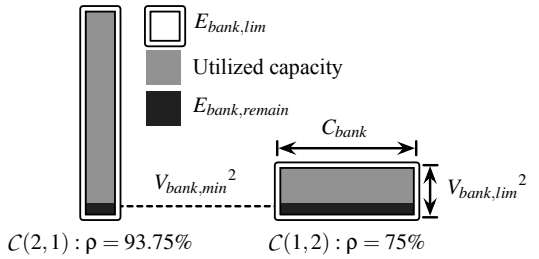

Fig. 8. Capacity utilization (ρ) of two configurations of a two-cell bank when $V_{bank,min} = \frac{1}{2} \cdot V_{cell,lim}$. Note that the vertical length is proportional to the square of voltage so that the area is proportional to the energy capacity.

conversion efficiency if the voltage range is chosen elaborately, but there is no explicit clue for setting the voltage range. Furthermore, the current which also affects the conversion efficiency is not considered for reconfiguration in the previous work. The proposed method exhibits a better efficiency since it considers the conversion efficiency for the reconfiguration taking the voltage and current into account.

B. Capacity Utilization

As discussed in Section III-C, the capacity utilization is also an important metric that determines the capital cost of an EES bank. We analyze the capacity utilization improvement by the proposed reconfiguration method. From (10) and (16), the remaining energy $E_{bank,remain}$ of a configuration $\mathcal{C}(m,n)$ when $V_{bank} = V_{bank,min}$ is

$$E_{bank,remain} = \frac{1}{2} \cdot \frac{n}{m} \cdot C_{cell} \cdot {V_{bank,min}}^2. \tag{25}$$

From (9), (10), (21), and that $N = m \cdot n$,

$$\rho = 1 - \left(\frac{\min\left(V_{bank,min}, m \cdot V_{cell,lim}\right)}{m \cdot V_{cell,lim}} \right)^2. \tag{26}$$

This implies that a reconfiguration in a way that increases m improves the capacity utilization. Fig. 8 is an example that graphically shows how the capacity utilization is improved by the reconfiguration. Here, $N = 2$, and two configurations $\mathcal{C}(2,1)$ and $\mathcal{C}(1,2)$ are available. The horizontal and vertical lengths of the box are proportional to the capacitance and square of the voltage, respectively, and so the area is proportional to the energy. Reconfiguration changes the way to store the same amount of energy; either in higher voltage and smaller capacitance (switching to a more series configuration), or in lower voltage and larger capacitance (switching to a more parallel configuration). Therefore, when the bank is deeply depleted and V_{bank} is near $V_{bank,min}$, we can maximize the capacity utilization by reconfiguring the bank to a configuration with the maximum m, that is, N.

VI. Experimental Results

In the experiments, we demonstrate that the proposed EES bank reconfiguration method improves the cycle efficiency and capacity utilization of an EES bank. Throughout this section, we use a supercapacitor bank consisting of capacitors with $C_{cell} = 100$ F and $V_{cell,lim} = 2.5$ V.

First, we demonstrate the energy efficiency improvement of the proposed EES bank reconfiguration method (GBRA) compared with two baselines: i) fixed EES bank configurations (Fixed), and ii) voltage variation-constraint (VVC) reconfiguration. The VVC reconfiguration method limits the bank voltage variation by switching the configuration when the bank voltage goes out of the given voltage range. We set the range of bank voltage to $\frac{1}{2} \cdot V_{cti} \le V_{bank} \le \frac{3}{2} \cdot V_{cti}$ for the VVC reconfiguration in the experiment. We assume a low minimum bank voltage constraint of $V_{bank,min} = 1.25$ V to minimize the effect of the capacity utilization limit.

We first demonstrate that the constant-power cycle efficiency η_{cyc} discussed in Section III-C, is improved by the proposed reconfiguration method. Fig. 9 shows the constant-power cycle efficiency of a 360-cell bank according to $P_{cti,cyc}$ ranging from 6 to 600 W, when $V_{cti} = 30$ V.

We can see that the proposed GBRA reconfiguration exhibits the best cycle efficiency for the all range by the timely efficiency-aware reconfiguration. On the other hand, the cycle efficiency of the VVC reconfiguration is lower than that of the GBRA reconfiguration, especially when the input/output power $P_{cti,cyc}$ is large. This is because the efficiency degradation due to the input and output voltage difference is escalated as the current increases. Fig. 9 also shows the cycle efficiency of the three fixed configurations: $\mathcal{C}(10,36)$, $\mathcal{C}(60,6)$, and $\mathcal{C}(180,2)$. The cycle efficiencies of the fixed configurations are not as high as that of the proposed GBRA reconfiguration in the all range of $P_{cti,cyc}$. The cycle efficiency improvement is up to 21% compared with the VVC reconfiguration and up to 108% compared with the fixed configurations in the range of 6–600 W. We can see from Fig. 9 that the cycle efficiency for larger $P_{cti,cyc}$ is optimal when the configuration has more cells in series. This is because a low bank voltage results in an excessively large current for larger $P_{cti,cyc}$, and induces a large P_{cdct} loss. In contrast, the P_{sw} loss becomes dominant for the high bank voltage cases. This clearly shows that finding the optimal configuration is not straightforward.

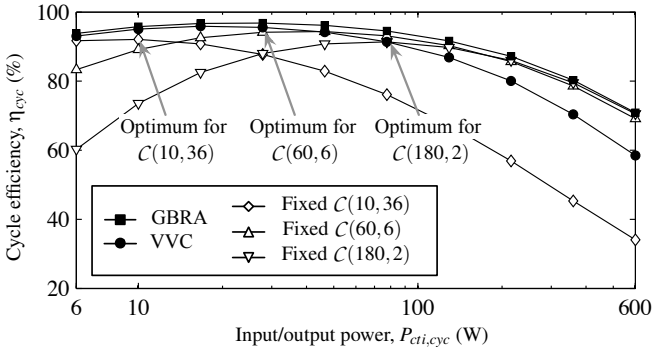

Fig. 9. Constant-power cycle efficiency comparison for different input/output power values of a 360-cell bank. CTI voltage (V_{cti}) is 30 V.

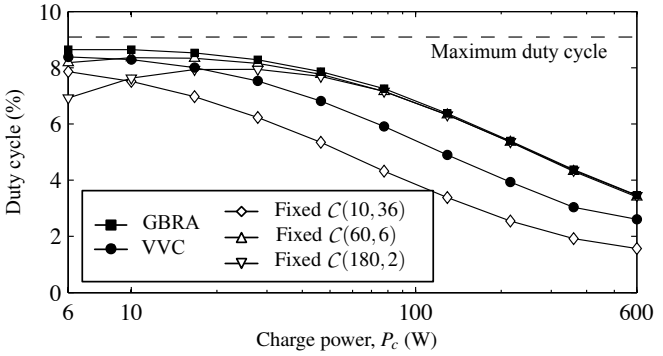

Fig. 10. Duty cycle for a high-current pulsed load of a 360-cell bank when discharge power (P_d) is 10 times higher than charge power (P_c). CTI voltage (V_{cti}) is 30 V.

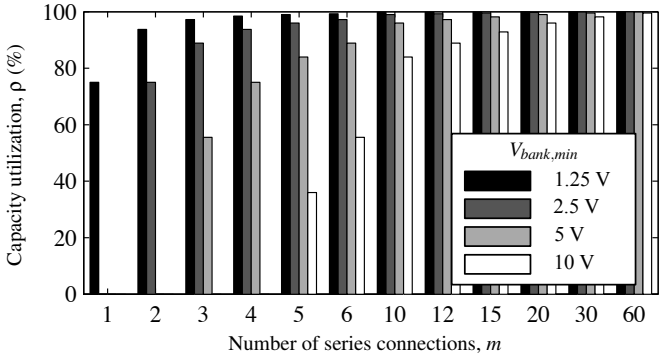

Fig. 11. Capacity utilization (ρ) for different number of series connections (m) and the minimum bank voltage requirement ($V_{bank,min}$).

Next, we demonstrate the energy efficiency improvement with a varying power input and output, which is more realistic for practical HEES systems. We charge the bank with a low input power until it is fully charged, and then discharge it with a high output power until it is fully depleted. The discharge power P_d is 10 times higher than the charge power P_c, and therefore the maximum duty cycle, which is possible only when the cycle efficiency is 100%, is $\frac{1}{10+1} = 9.1\%$. Fig. 10 shows the duty cycle of a 360-cell bank for P_c ranging from 6 to 600 W, when $V_{cti} = 30$ V. This result also shows that the proposed GBRA reconfiguration exhibits higher energy efficiency even for a realistic high-power pulsed load demand, compared with the VVC reconfiguration and fixed configurations. The duty cycle improvement is by up to 44% compared with the VVC reconfiguration and by up to 127% compared with the fixed configurations in the range of 6–600 W input power.

We demonstrate the capacity utilization for different m and $V_{bank,min}$ values in Fig. 11. As seen in (26), the capacity utilization is dependent on m but not on n. We can see that the capacity utilization increases as m increases. This result clearly shows the motivation of dynamic reconfiguration to fully utilize the capacity. By dynamically increasing the number of series connections, m, when the bank is almost depleted, we can extract more energy from the bank. For example, when $V_{bank,min} = 10$ V, using a fixed configuration with $m = 10$ results in 84% of capacity utilization. These imply that 16% of the capital cost to purchase and dispose the EES elements is wasted without substantial capacity increase. The capital cost loss is reduced to less than 1% when the EES bank can be reconfigured to $m = 60$.

VII. Conclusions

This paper is the first paper to introduce a reconfiguration of the energy storage banks in hybrid electric energy storage (HEES) systems aiming at cycle efficiency and capacity utilization improvements. The cycle efficiency and capacity utilization directly affect the operational cost and the capital cost of the HEES system, respectively. We developed the general balanced reconfiguration architecture (GBRA) for EES banks reconfiguration, and discussed important properties of the GBRA-based reconfigurable EES banks. We presented a dynamic reconfiguration algorithm composed of an online and an offline algorithm considering the conversion efficiency of the power converters. We applied the proposed reconfiguration method to supercapacitor banks, and demonstrated that the cycle efficiency could be improved by up to 108% for a constant power usage profile, whereas the pulse duty cycle was improved by up to 127% for a high-current pulsed power profile. The capacity utilization analysis showed that the dynamic reconfiguration of EES banks improves the utilization, which in turn reduces the capital cost of the HEES systems.

Acknowledgements

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